

# 2 Mbit ROM + 1 Mbit / 2Mbit / 256 Kbit SRAM ROM/RAM Combo

SST30VR021 / SST30VR022 / SST30VR023



Data Sheet

## FEATURES:

- **ROM + SRAM ROM/RAM Combo**
  - SST30VR021: 256K x8 ROM + 128K x8 SRAM
  - SST30VR022: 256K x8 ROM + 256K x8 SRAM
  - SST30VR023: 256K x8 ROM + 32K x8 SRAM
- **ROM/RAM combo on a monolithic chip**
- **Equivalent ComboMemory (Flash + SRAM):**  
SST31LF021E for code development and pre-production
- **Wide Operating Voltage Range: 2.7-3.3V**
- **Chip Access Time**
  - SST30VR022 70 ns
  - SST30VR021/023 500 ns
- **Low Power Dissipation:**
  - Standby: 3  $\mu$ W (Typical)
  - Operating: 10 mW (Typical)
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Outputs**
- **Packages Available**
  - 32-pin TSOP (8mm x14mm)

## PRODUCT DESCRIPTION

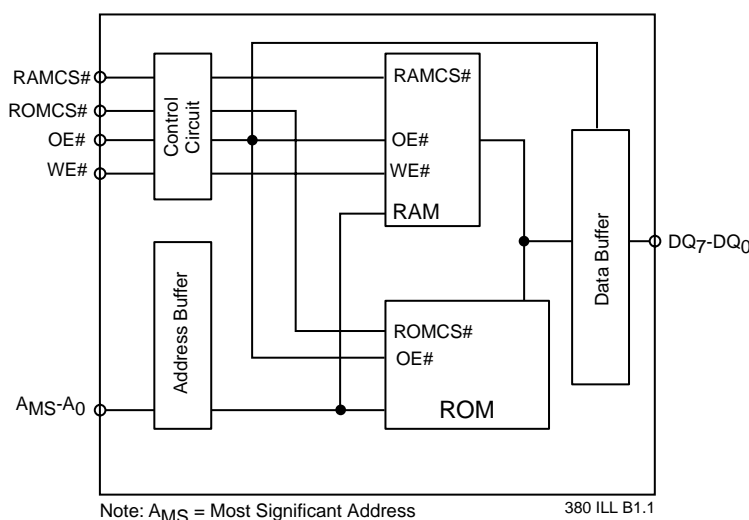
The SST30VR021/022/023 are ROM/RAM combo chips consisting of 2 Mbit Read Only Memory organized as 256 KBytes and Static Random Access Memory organized as 128, 256, and 32 KBytes.

The device is fabricated using SST's advanced CMOS low power process technology.

The SST30VR021/022/023 has an output enable input for precise control of the data outputs. It also has two (2) separate chip enable inputs for selection of either RAM or ROM and for minimizing current drain during power-down mode.

The SST30VR021/022/023 is particularly well suited for use in low voltage (2.7-3.3V) supplies such as pagers, organizers and other handheld applications.

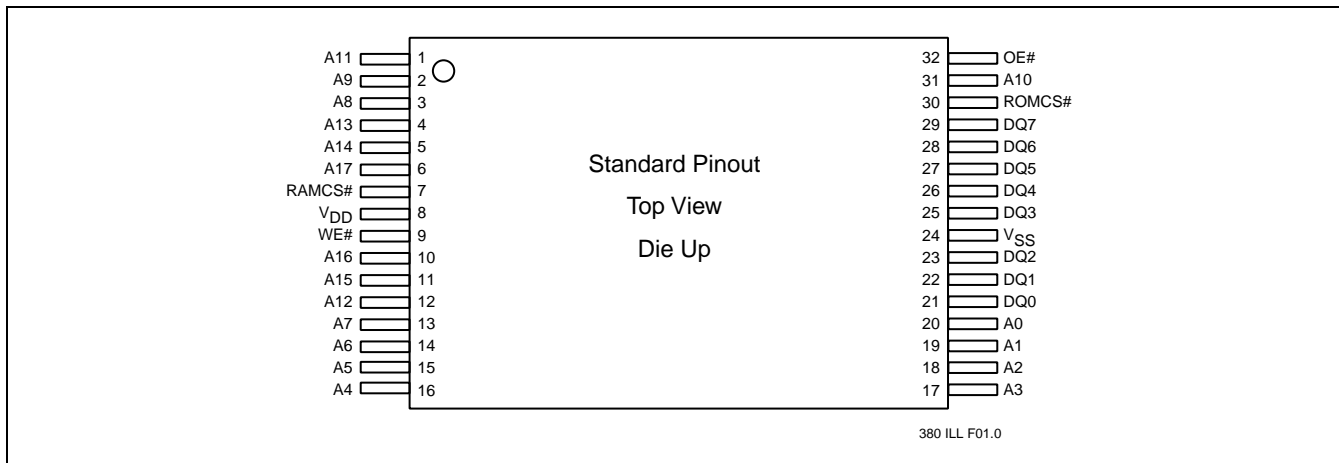
### FUNCTIONAL BLOCK DIAGRAM





**2 Mbit ROM + 1 Mbit / 2Mbit / 256 Kbit SRAM  
ROM/RAM Combo  
SST30VR021 / SST30VR022 / SST30VR023**

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**FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN TSOP**

**TABLE 1: PIN DESCRIPTION**

Symbol	Pin Name
$A_{MS}^1-A_0$	Address Inputs, for ROM: $A_{MS} = A_{17}$ , for RAM: $A_{MS} = A_{16}$ for SST30VR021 $A_{17}$ for SST30VR022 $A_{14}$ for SST30VR023
WE#	Write Enable Input
OE#	Output Enable
RAMCS#	RAM Enable Input
ROMCS#	ROM Enable Input
DQ <sub>7</sub> -DQ <sub>0</sub>	Data Input/Output
V <sub>DD</sub>	Power Supply
V <sub>SS</sub>	Ground

1.  $A_{MS}$  = Most significant address

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**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature ..... -20°C to +85°C  
 Storage Temperature ..... -65°C to +150°C  
 Voltage on Any Pin Relative to V<sub>SS</sub> ..... -0.5V to V<sub>DD</sub> + 0.5V  
 Voltage on V<sub>DD</sub> Supply Relative to V<sub>SS</sub> ..... -0.5V to 4.0V  
 Power Dissipation..... 1.0W  
 Soldering Temperature (10 Seconds Lead Only) ..... 260°C

**OPERATING RANGE**

Range	Ambient Temp	V <sub>DD</sub>
Commercial	0°C to +70°C	2.7-3.3V
Extended	-20°C to +85°C	2.7-3.3V

**AC CONDITIONS OF TEST**

Input Pulse Level.....	0-V <sub>DD</sub>
Input & Output Timing Reference Levels.....	V <sub>DD</sub> /2
Input Rise/Fall Time.....	5 ns
Output Load.....	C <sub>L</sub> = 30 pF for 70 ns
Output Load.....	C <sub>L</sub> = 100 pF for 500 ns

**TABLE 2: RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Units
V <sub>DD</sub>	Supply Voltage	2.7	3.3	V
V <sub>SS</sub>	Ground	0	0	V
V <sub>IH</sub>	Input High Voltage	2.4	V <sub>DD</sub> + 0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.3	0.3	V

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**TABLE 3: DC OPERATING CHARACTERISTICS**

Symbol	Parameter	V <sub>DD</sub> = 3.0 ± 0.3V			Test Conditions
		Min	Max	Units	
I <sub>DD1</sub>	ROM Operating Supply Current		4.0+1.1(f) <sup>1</sup>	mA	ROMCS#=V <sub>IL</sub> , RAMCS#=V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> =Opens
I <sub>DD2</sub>	RAM Operating Supply Current		2.5+1(f) <sup>1</sup>	mA	ROMCS#=V <sub>IH</sub> , RAMCS#=V <sub>IL</sub> , I <sub>I/O</sub> =Opens
I <sub>SB</sub>	Standby V <sub>DD</sub> Current		10	µA	ROMCS#≥V <sub>DD</sub> -0.2V, RAMCS#≥V <sub>DD</sub> -0.2V V <sub>IN</sub> ≥V <sub>DD</sub> -0.2V or V <sub>IN</sub> ≤0.2V
I <sub>LI</sub>	Input Leakage Current	-1	1	µA	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>DD</sub>
I <sub>LO</sub>	Output Leakage Current	-1	1	µA	ROMCS#=RAMCS#=V <sub>IH</sub> or OE#=V <sub>IH</sub> or WE#=V <sub>IL</sub> , V <sub>I/O</sub> =V <sub>SS</sub> to V <sub>DD</sub>
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 1.0 mA
V <sub>OH</sub>	Output High Voltage	2.2		V	I <sub>OH</sub> = -0.5 mA

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1. f = Frequency of operation (MHz) = 1/cycle time



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TABLE 4: CAPACITANCE ( $T_a = 25^\circ\text{C}$ ,  $f=1\text{ Mhz}$ )

Parameter	Description	Test Condition	Maximum
$C_{I/O}^1$	I/O Pin Capacitance	$V_{I/O} = 0\text{V}$	8 pF
$C_{IN}^1$	Input Capacitance	$V_{IN} = 0\text{V}$	6 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

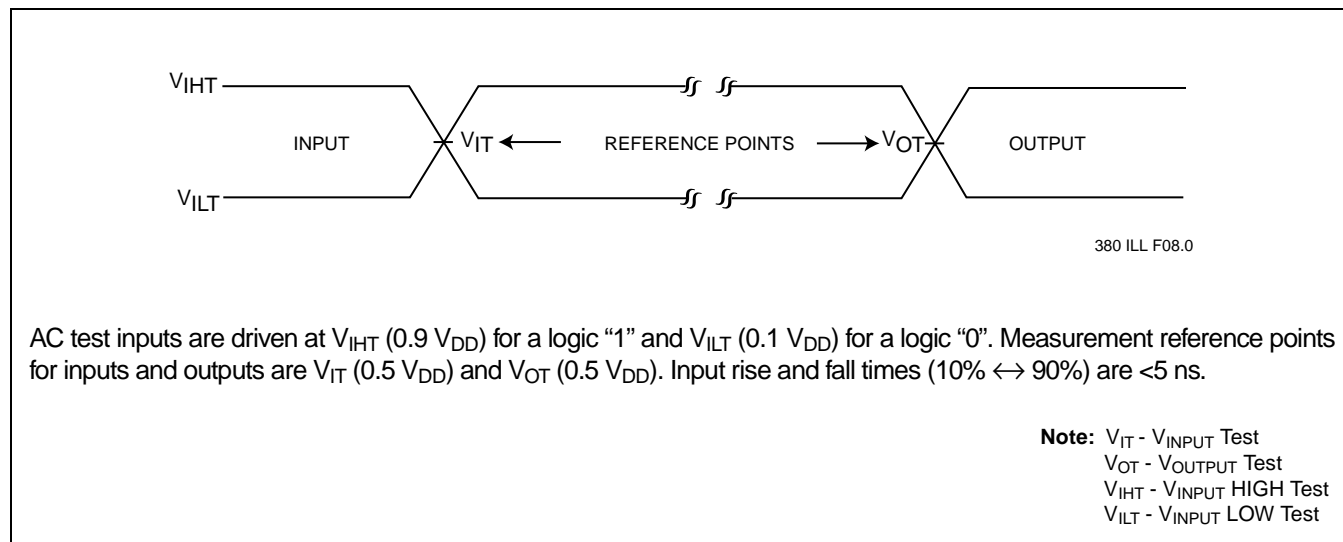


FIGURE 2: AC INPUT/OUTPUT REFERENCE WAVEFORMS

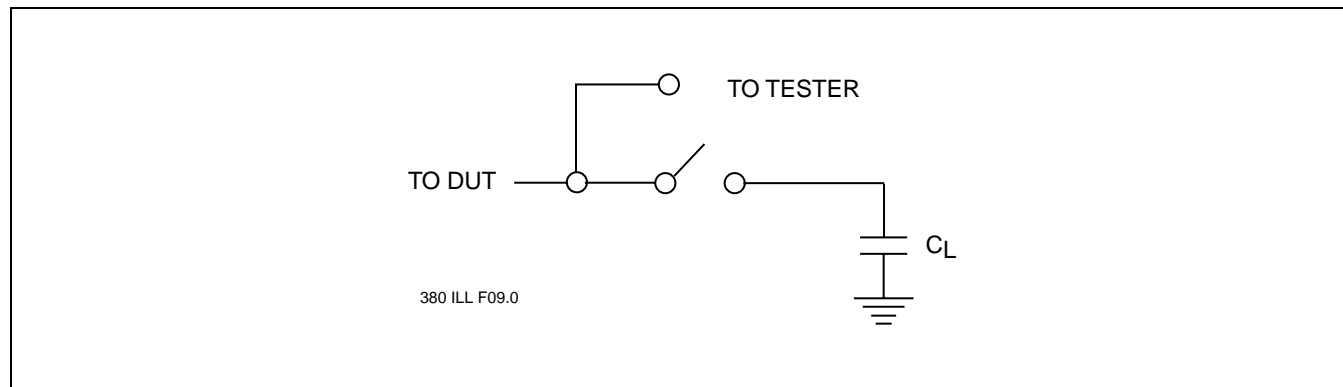


FIGURE 3: A TEST LOAD EXAMPLE



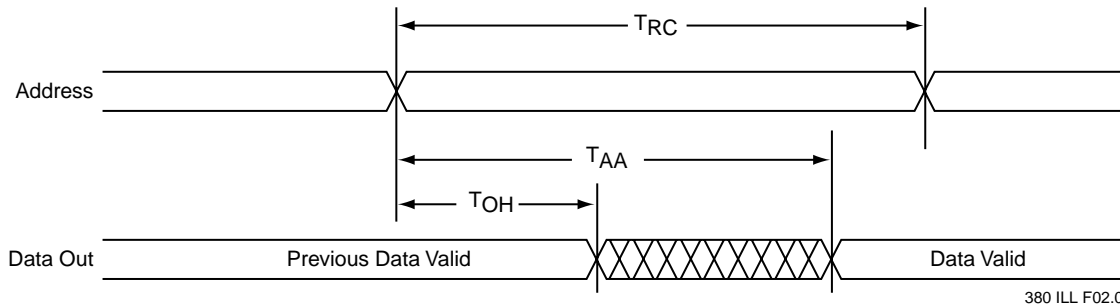
AC CHARACTERISTICS

I. ROM Operation

TABLE 5: READ CYCLE TIMING PARAMETERS  $V_{DD} = 3.0V \pm 0.3$

Symbol	Parameter	SST30VR022-70		SST30VR021/023-500		Units
		Min	Max	Min	Max	
$T_{RC}$	Read Cycle Time	70		500		ns
$T_{AA}$	Address Access Time		70		500	ns
$T_{CO}$	Chip Select to Output		70		500	ns
$T_{OE}$	Output Enable to Valid Output		35		250	ns
$T_{LZ}$	Chip Select to Low-Z Output	0		25		ns
$T_{OLZ}$	Output Enable to Low-Z Output	0		25		ns
$T_{HZ}$	Chip Disable to High-Z Output		25		30	ns
$T_{OHZ}$	Output Disable to High-Z Output		25		30	ns
$T_{OH}$	Output Hold from Address Change	10		15		ns

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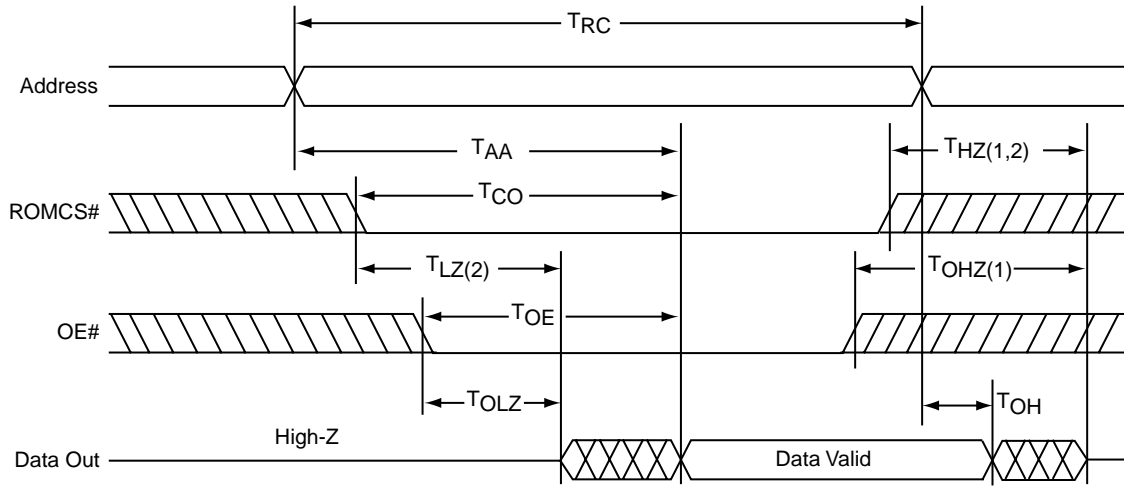
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FIGURE 4: ROM READ CYCLE TIMING DIAGRAM (ADDRESS CONTROLLED) (ROMCS# = OE# =  $V_{IL}$ )



2 Mbit ROM + 1 Mbit / 2Mbit / 256 Kbit SRAM  
ROM/RAM Combo  
SST30VR021 / SST30VR022 / SST30VR023

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- Notes:
1.  $T_{HZ}$  and  $T_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are referenced to the  $V_{OH}$  or  $V_{OL}$ .
  2. At any given temperature and voltage condition  $T_{HZ}(\max)$  is less than  $T_{LZ}(\min)$  both for a given device and from device to device.

FIGURE 5: ROM READ CYCLE TIMING DIAGRAM (ROMCS# & OE# CONTROLLED)

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ROM/RAM Combo  
SST30VR021 / SST30VR022 / SST30VR023**



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**II. SRAM Operation (ROMCS# = V<sub>IH</sub>)**

**TABLE 6: READ CYCLE TIMING PARAMETERS V<sub>DD</sub> = 3.0V±0.3**

Symbol	Parameter	SST30VR022-70		SST30VR021/023-500		Units
		Min	Max	Min	Max	
T <sub>RC</sub>	Read Cycle Time	70		500		ns
T <sub>AA</sub>	Address Access Time		70		500	ns
T <sub>CO</sub>	Chip Select to Output		70		500	ns
T <sub>OE</sub>	Output Enable to Valid Output		35		250	ns
T <sub>LZ</sub>	Chip Select to Low-Z Output	0		25		ns
T <sub>HZ</sub>	Chip Disable to High-Z Output		25		30	ns
T <sub>OHZ</sub>	Output Disable to High-Z Output		25		30	ns
T <sub>OH</sub>	Output Hold from Address Change	10		15		ns

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**TABLE 7: WRITE CYCLE TIMING PARAMETERS V<sub>DD</sub> = 3.0V±0.3**

Symbol	Parameter	SST30VR022-70		SST30VR021/023-500		Units
		Min	Max	Min	Max	
T <sub>WC</sub>	Write Cycle Time	70		500		ns
T <sub>CW</sub>	Chip Select to End-of-Write	60		365		ns
T <sub>AW</sub>	Address Valid to End-of-Write	60		375		ns
T <sub>AS</sub>	Address Set-up Time	0		0		ns
T <sub>WP</sub>	Write Pulse Width	60		375		ns
T <sub>WR</sub>	Write Recovery Time	0		0		ns
T <sub>WHZ</sub>	Write to Output High-Z		30		80	ns
T <sub>DW</sub>	Data to Write Time Overlap	30		200		ns
T <sub>DH</sub>	Data Hold from Write Time	0		0		ns
T <sub>OW</sub>	End Write to Output Low-Z	0		15		ns

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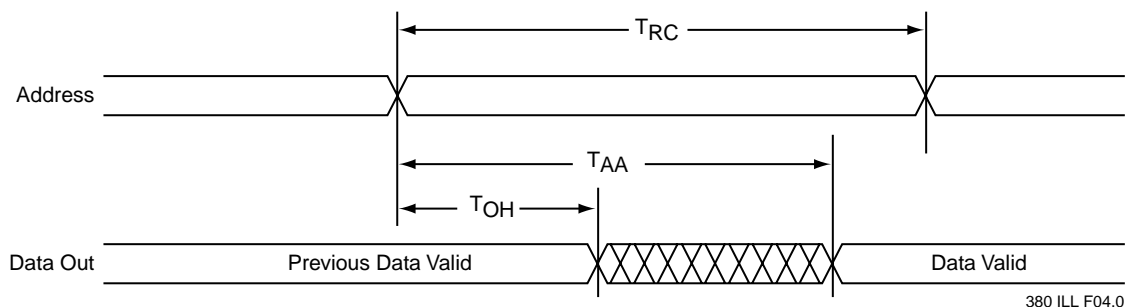
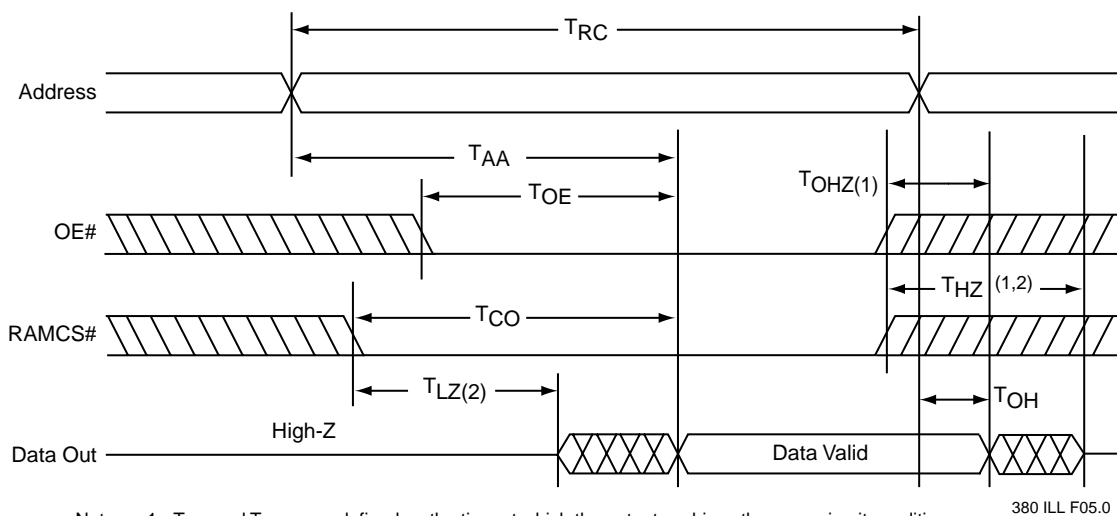


FIGURE 6: SRAM READ CYCLE TIMING DIAGRAM (ADDRESS CONTROLLED) (OE# = RAMCS# = V<sub>IL</sub>, WE# = V<sub>IH</sub>)



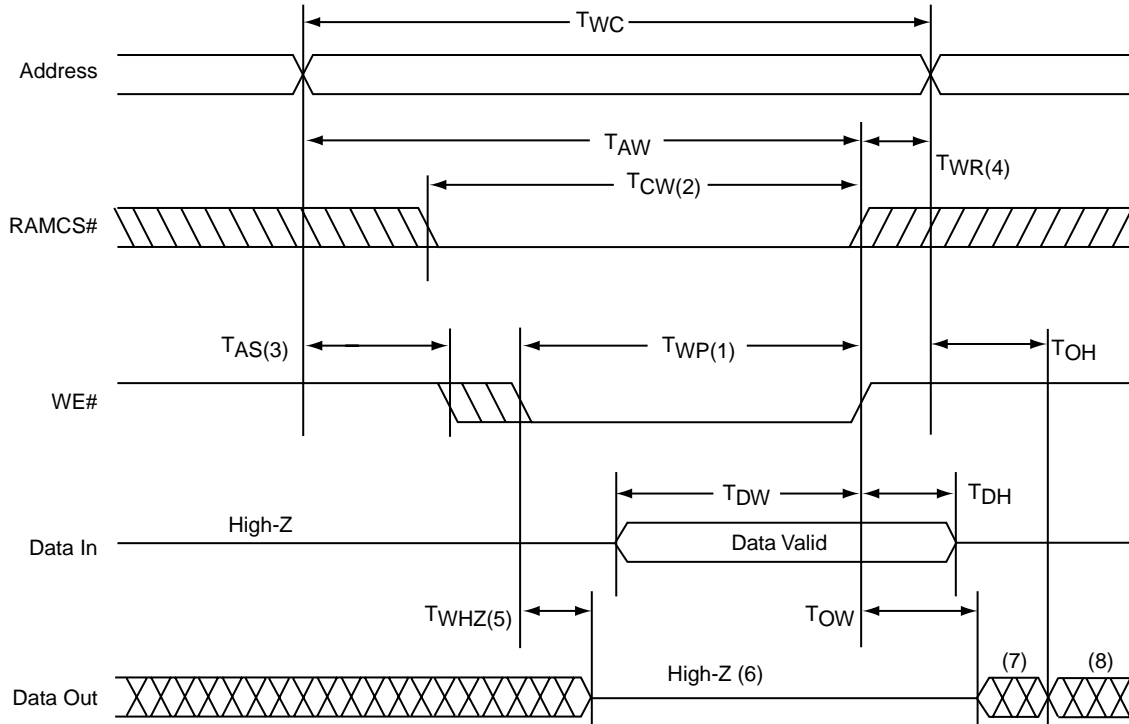
- Notes:
1. T<sub>HZ</sub> and T<sub>OZH</sub> are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V<sub>OH</sub> or V<sub>OL</sub>.
  2. At any given temperature and voltage condition T<sub>HZ</sub>(max) is less than T<sub>LZ</sub>(min) both for a given device and from device to device.
  3. WE# is high for Read cycle.
  4. Address valid prior to coincidence with RAMCS# transition low.

FIGURE 7: SRAM READ CYCLE TIMING DIAGRAM (OE# OR RAMCS# CONTROLLED)

**2 Mbit ROM + 1 Mbit / 2Mbit / 256 Kbit SRAM**  
**ROM/RAM Combo**  
**SST30VR021 / SST30VR022 / SST30VR023**



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- Notes:
1. A write occurs during the overlap ( $T_{WP}$ ) of a low RAMCS# and low WE#. A write begins at the latest transition among RAMCS# going low and WE# going low; a write ends at the earliest transition among RAMCS# going high and WE# going high.  $T_{WP}$  is measured from the beginning of write to the end of write.
  2.  $T_{CW}$  is measured from the later of RAMCS# going low to the end of write.
  3.  $T_{AS}$  is measured from the address valid to the beginning of write.
  4.  $T_{WR}$  is measured from the end of write to the address change.
  5. If RAMCS#, WE# are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
  6. If RAMCS# goes low simultaneously with WE# going low or after WE# going low, the outputs remain high impedance state.
  7.  $D_{OUT}$  is the same phase of the latest written data in this write cycle.
  8.  $D_{OUT}$  is the read data of new address
  9.  $ROMCS\# = V_{IH}$

**FIGURE 8: SRAM WRITE CYCLE TIMING DIAGRAM**

**TABLE 8: FUNCTIONAL DESCRIPTION/TRUTH TABLE**

Address Inputs	ROMCS# <sup>1</sup>	RAMCS# <sup>1</sup>	WE#	OE#	DQ <sub>0</sub> -DQ <sub>7</sub>	
X	H	H	X <sup>2</sup>	X <sup>2</sup>	Z	Standby
A <sub>17</sub> -A <sub>0</sub>	L	H	X <sup>2</sup>	H	Z	Output Floating
A <sub>17</sub> -A <sub>0</sub>	L	H	X <sup>2</sup>	L	Dout	ROM Read
Only A <sub>MS</sub> <sup>3</sup> -A <sub>0</sub> are valid <sup>4</sup>	H	L	H	H	Z	Output Floating
Only A <sub>MS</sub> <sup>3</sup> -A <sub>0</sub> are valid <sup>4</sup>	H	L	H	L	Dout	RAM Read
Only A <sub>MS</sub> <sup>3</sup> -A <sub>0</sub> are valid <sup>4</sup>	H	L	L	H	Din	RAM Write

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1. It is forbidden for ROMCS# pin and RAMCS# pin to be "0" at the same time
2. X means Don't Care.
3. A<sub>MS</sub> = A<sub>16</sub> for SST30VR021, A<sub>17</sub> for SST30VR022, and A<sub>14</sub> for SST30VR023
4. For SST30VR021: A<sub>17</sub> must be fixed to "L" or "H"  
 For SST30VR023: A<sub>15</sub>, A<sub>16</sub>, and A<sub>17</sub> must be fixed to "L" or "H"

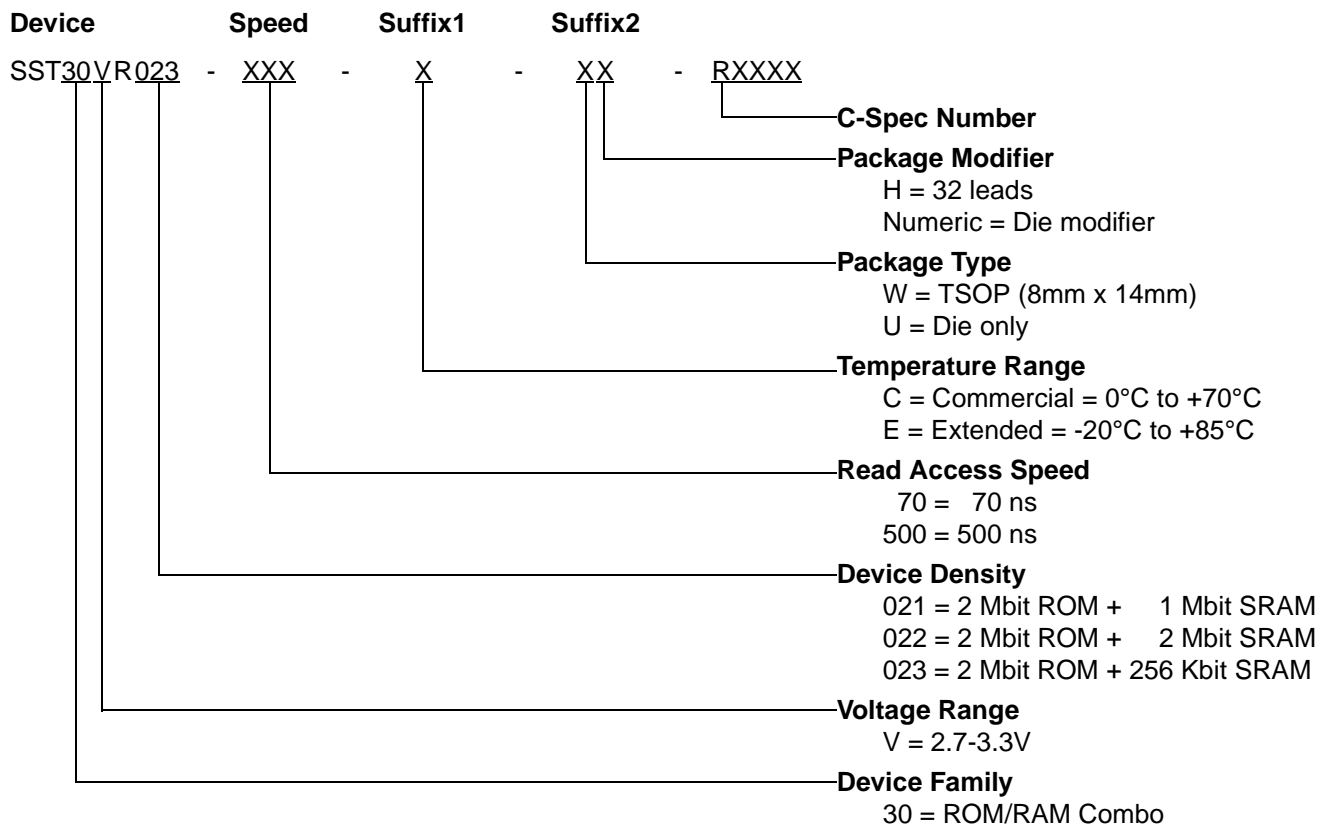


## 2 Mbit ROM + 1 Mbit / 2Mbit / 256 Kbit SRAM

### ROM/RAM Combo

### SST30VR021 / SST30VR022 / SST30VR023

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#### SST30VR021 Valid combinations

SST30VR021-500-C-WH  
SST30VR021-500-C-U1  
SST30VR021-500-E-WH

#### SST30VR022 Valid combinations

SST30VR022-70-C-WH  
SST30VR022-70-C-U1  
SST30VR022-70-E-WH

#### SST30VR023 Valid combinations

SST30VR023-500-C-WH  
SST30VR023-500-C-U1  
SST30VR023-500-E-WH

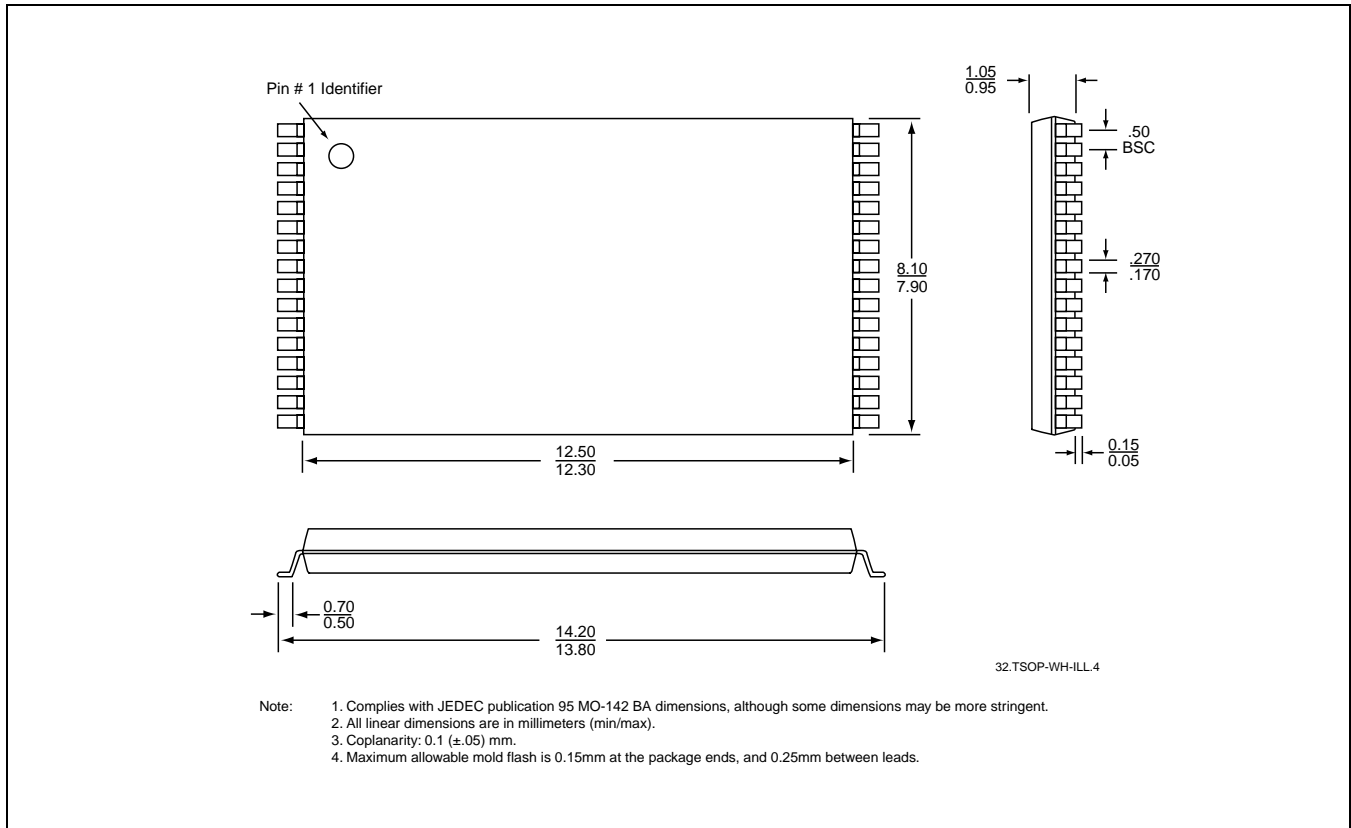
**Example:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

**2 Mbit ROM + 1 Mbit / 2Mbit / 256 Kbit SRAM  
ROM/RAM Combo  
SST30VR021 / SST30VR022 / SST30VR023**



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**PACKAGING DIAGRAMS**



**32-PIN THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM  
SST PACKAGE CODE: WH**



**2 Mbit ROM + 1 Mbit / 2Mbit / 256 Kbit SRAM  
ROM/RAM Combo  
SST30VR021 / SST30VR022 / SST30VR023**

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