

# 4 Megabit Flash + 1 Megabit SRAM ComboMemory

## SST31LF041A



Advance Information

### FEATURES:

- **Organized as 512K x8 Flash + 128K x8 SRAM**
- **Single 3.0-3.6V Read and Write Operations**
- **Concurrent Operation**
  - Read from or Write to SRAM while Erase/Program Flash
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 10 mA (typical) for Flash Read and 20 mA (typical) for SRAM Read/Write
  - Standby Current: 10  $\mu$ A (typical)
- **Flash Sector-Erase Capability**
  - Uniform 4 KByte sectors
- **Fast Read Access Times:**
  - Flash: 300 ns
  - SRAM: 300 ns
- **Latched Address and Data for Flash**
- **Flash Fast Erase and Byte-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Bank-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14  $\mu$ s (typical)
  - Bank Rewrite Time: 8 seconds (typical)
- **Flash Automatic Erase and Program Timing**
  - Internal  $V_{PP}$  Generation
- **Flash End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Package Available**
  - 32-Pin TSOP (8mm x 13.4mm)

### PRODUCT DESCRIPTION

The SST31LF041A is a 512K x8 CMOS flash memory bank combined with a 128K x8 CMOS SRAM memory bank manufactured with SST's proprietary, high performance SuperFlash technology. It is different than the SST31LF041 where BES# and OE# are shared to further take advantage of Flash and SRAM integration in a smaller size package. The SST31LF041A device writes (Flash or SRAM) with a 3.0-3.6V power supply. The monolithic SST31LF041A device is available in a 32-pin TSOP package where BES# and OE# shares pin 32.

Featuring high performance Byte-Program, the flash memory bank provides a maximum Byte-Program time of 20  $\mu$ sec. The entire flash memory bank can be erased and programmed byte-by-byte in typically 8 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent flash write, the SST31LF041A device has on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST31LF041A device is offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST31LF041A operates as two independent memory banks with respective bank enable signals. The SRAM and Flash memory banks are superimposed in the same memory address space. Both memory banks share common address lines, data lines, WE# and OE#. The memory bank selection is done by memory bank enable

signals. The SRAM bank enable signal, BES# selects the SRAM bank and the flash memory bank enable signal, BEF# selects the flash memory bank. The WE# signal has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The SDP command sequence protects the data stored in the flash memory bank from accidental alteration.

The SST31LF041A provides the added functionality of being able to simultaneously read from or write to the SRAM bank while erasing or programming in the flash memory bank. The SRAM memory bank can be read or written while the flash memory bank performs Sector-Erase, Bank-Erase, or Byte-Program concurrently. All flash memory Erase and Program operations will automatically latch the input address and data signals and complete the operation in background without further input stimulus requirement. Once the internally controlled Erase or Program cycle in the flash bank has commenced, the SRAM bank can be accessed for Read or Write.

The SST31LF041A device is suited for applications that use both nonvolatile flash memory and volatile SRAM memory to store code or data. For all system applications, the SST31LF041A device significantly improves performance and reliability, while lowering power consumption, when compared with multiple chip solutions. The SST31LF041A inherently uses less energy during Erase and Program than alternative flash technologies. When programming a flash device, the total energy



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consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. The monolithic ComboMemory eliminates redundant functions when using two separate memories of similar architecture; therefore, reducing the total power consumption.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

The SST31LF041A device also improves flexibility by using a single package and a common set of signals to perform functions previously requiring two separate devices. To meet high density, surface mount requirements, the SST31LF041A device is offered in a 32-pin package. See Figure 1 for the pinouts.

### Device Operation

The ComboMemory uses BES# and BEF# to control operation of either the SRAM or the flash memory bank. Bus contention is eliminated as the monolithic device will not recognize both bank enables as being simultaneously active. If both bank enables are asserted (i.e., BEF# and BES# are both low), the BEF# will dominate while the BES# is ignored and the appropriate operation will be executed in the flash memory bank. SST does not recommend that both bank enables be simultaneously asserted. All other address, data, and control lines are shared; which minimizes power consumption and area. The device goes into standby when both bank enables are raised to  $V_{IHC}$ .

BES# and OE# shares pin 32. During SRAM operation, pin 32 will function as BES#. During flash operation, pin 32 will function as OE#. When pin 32 (OE#/BES#) is high, the data bus is in high impedance state.

### SRAM Operation

With BES# low and BEF# high, the SST31LF041A operates as a 128K x 8 CMOS SRAM, with fully static operation requiring no external clocks or timing strobes. The SRAM is mapped into the first 128 KByte address space of the device. Read and Write cycle times are equal. See Table 4 for SRAM operation modes selection.

### SRAM Read

The SRAM Read operation of the SST31LF041A is controlled by OE#/BES#. BES# is used for SRAM bank

selection. Since OE# and BES# are shared, pin 32 has to be low with WE# high, for the system to obtain data from the outputs. When BES# and BEF# are high, both memory banks are deselected. See Figure 2 for Read Cycle Timing.

### SRAM Write

The SRAM Write operation of the SST31LF041A is controlled by WE# and BES#, both have to be low for the system to write to the SRAM. BES# is used for SRAM bank selection. During the Byte-Write operation, the addresses and data are referenced to the rising edge of either BES# or WE#, whichever occurs first. The Write time is measured from the last falling edge to the first rising edge of BES# and WE#. Refer to the Write cycle timing diagram, Figure 3. OE# is "don't care" for SRAM Write operations. See Figure 3 for Write Cycle Timing, where BES# and OE# shares pin 32.

### Flash Operation

With BEF# active, the SST31LF041A operates as a 512K x 8 flash memory. The flash memory bank is read using the common address lines, data lines, WE# and OE#. Erase and Program operations are initiated with the JEDEC standard SDP command sequences. Address and data are latched during the SDP commands and internally timed Erase and Program operations. BES# and OE# share pin 32. During flash operation, pin 32 functions as OE#. See Table 3 for flash operation modes selection.

### Flash Read

The Read operation of the SST31LF041A device is controlled by BEF# and OE#, both have to be low, with WE# high, for the system to obtain data from the outputs. BEF# is used for flash memory bank selection. When BEF# and OE# are high, both banks are deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. Refer to the Read cycle timing diagram (Figure 4) for further details.

### Flash Erase/Program Operation

SDP commands are used to initiate the flash memory bank Program and Erase operations of the SST31LF041A. SDP commands are loaded to the flash memory bank using standard microprocessor write sequences. A command is loaded by asserting WE# low while keeping BEF# low and OE# high. The address is latched on the falling edge of WE# or BEF#, whichever occurs last. The data is latched on the rising edge of WE# or BEF#, whichever occurs first.



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#### Flash Byte-Program Operation

The flash memory bank of the SST31LF041A device is programmed on a byte-by-byte basis. The Program operation consists of three steps. The first step is the three-byte-load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed, within 20  $\mu$ s. See Figures 5 and 6 for WE# and BEF# controlled Program operation timing diagrams and Figure 16 for flowcharts. During the Program operation, the only valid Flash Read operations are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any SDP commands loaded during the internal Program operation will be ignored.

#### Flash Sector-Erase Operation

The Sector-Erase operation allows the system to erase the flash memory bank on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KBytes. The Sector-Erase operation is initiated by executing a six-byte-command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The address lines A18-A12 will be used to determine the sector address. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 9 for timing waveforms. Any SDP commands loaded during the Sector-Erase operation will be ignored.

#### Flash Bank-Erase Operation

The SST31LF041A flash memory bank provides a Bank-Erase operation, which allows the user to erase the entire flash memory bank array to the "1's" state. This is useful when the entire bank must be quickly erased. The Bank-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Bank-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or BEF# pulse, whichever occurs first. During the internal Erase operation, the only valid Flash Read operations are Toggle Bit and Data# Polling. See Table 5 for the command sequence,

Figure 10 for timing diagram, and Figure 19 for the flowchart. Any SDP commands loaded during the Bank-Erase operation will be ignored.

#### Flash Write Operation Status Detection

The SST31LF041A flash memory bank provides two software means to detect the completion of a flash memory bank Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ7 or DQ6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

#### Flash Data# Polling (DQ7)

When the SST31LF041A flash memory bank is in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce true data. The flash memory bank is then ready for the next operation. During internal Erase operation, any attempt to read DQ7 will produce a '0'. Once the internal Erase operation is completed, DQ7 will produce a '1'. The Data# Polling is valid after the rising edge of the fourth WE# (or BEF#) pulse for Program operation. For Sector or Bank-Erase, the Data# Polling is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 7 for Data# Polling timing diagram and Figure 17 for a flowchart.

#### Flash Toggle Bit (DQ6)

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The flash memory bank is then ready for the next operation. The Toggle Bit is valid after the rising edge of the fourth WE# (or BE#) pulse for Program operation. For Sector- or Bank-Erase, the Toggle Bit is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 8 for Toggle Bit timing diagram and Figure 17 for a flowchart.



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### Flash Memory Data Protection

The SST31LF041A flash memory bank provides both hardware and software features to protect nonvolatile data from inadvertent writes.

### Flash Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a Write cycle.

V<sub>DD</sub> Power Up/Down Detection: The Write operation is inhibited when V<sub>DD</sub> is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the Flash Write operation. This prevents inadvertent writes during power-up or power-down.

### Flash Software Data Protection (SDP)

The SST31LF041A provides the JEDEC approved Software Data Protection scheme for all flash memory bank data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence. The SST31LF041A device is shipped with the Software Data Protection permanently enabled. See Table 5 for the specific software command codes. During SDP command sequence, invalid SDP commands will abort the device to the Read mode, within TRC.

### Concurrent Read and Write Operations

The SST31LF041A provides the unique benefit of being able to read from or write to SRAM, while simultaneously erasing or programming the Flash. The device will ignore all SDP commands when an Erase or Program operation is in progress. This allows data alteration code to be executed from SRAM, while altering the data in Flash. The following table lists all valid states. SST does not recommend that both bank enables, BEF# and BES#, be simultaneously asserted.

CONCURRENT READ/WRITE STATE TABLE

Flash	SRAM
Program/Erase	Read
Program/Erase	Write

Note that Product Identification commands use SDP; therefore, these commands will also be ignored while an Erase or Program operation is in progress.

### Product Identification

The product identification mode identifies the device as the SST31LF041A and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware device ID Read operation is typically used by a programmer to identify the correct algorithm for the SST31LF041A flash memory bank. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 5P for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION TABLE

	Address	Data
Manufacturer's Code	0000H	BF H
Device Code	0001H	16 H

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### Product Identification Mode Exit/Reset

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software-reset command is ignored during an internal Program or Erase operation. See Table 5 for software command codes, Figure 12 for timing waveform and Figure 18 for a flowchart.

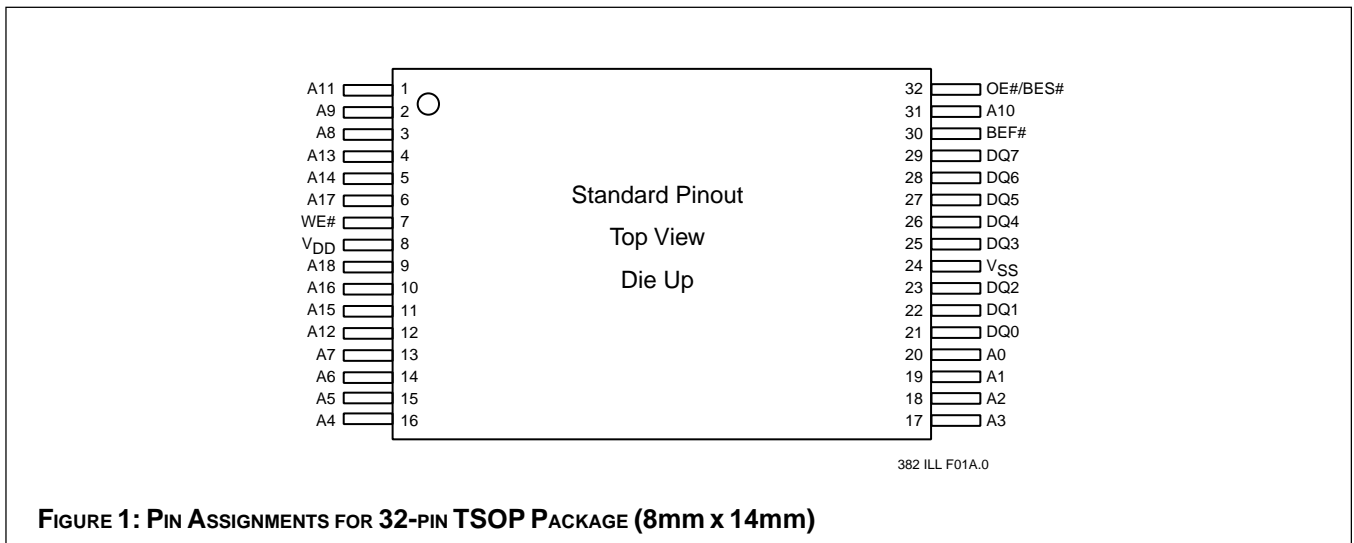
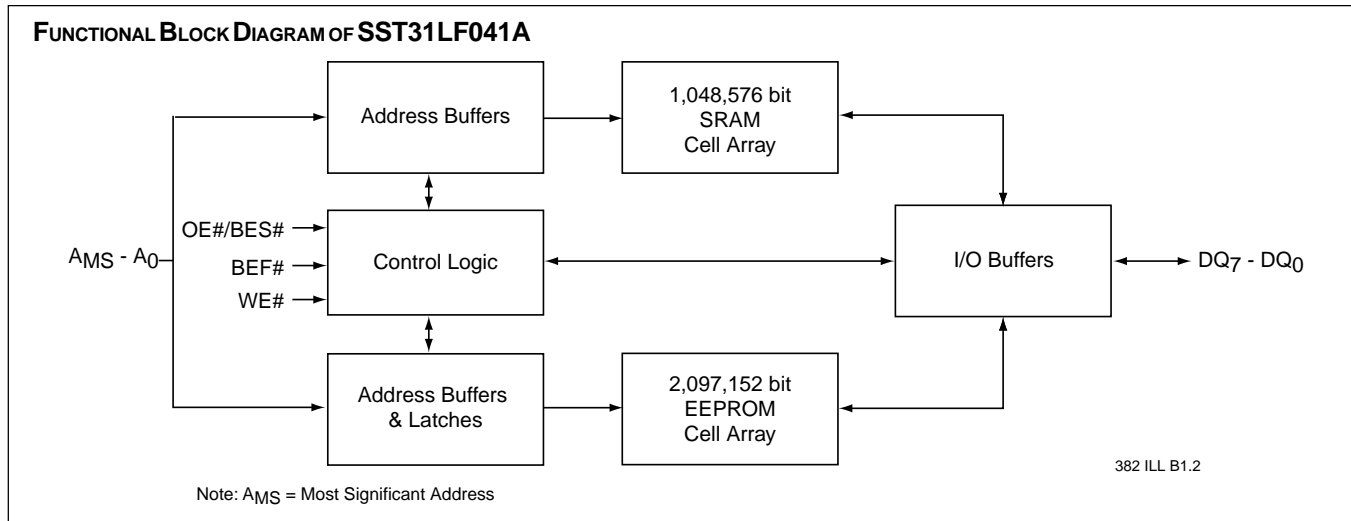
### Design Considerations

SST recommends a high frequency 0.1 μF ceramic capacitor to be placed as close as possible between V<sub>DD</sub> and V<sub>SS</sub>, e.g., less than 1 cm away from the V<sub>DD</sub> pin of the device. Additionally, a low frequency 4.7 μF electrolytic capacitor from V<sub>DD</sub> to V<sub>SS</sub> should be placed within 1 cm of the V<sub>DD</sub> pin.



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**FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN TSOP PACKAGE (8mm x 14mm)**

**TABLE 2: PIN DESCRIPTION**

Symbol	Pin Name	Functions
AMS-A0	Address Inputs	To provide memory addresses. During Flash Sector-Erase A18-A12 address lines will select the sector. A18-A0 to provide flash address, A16-A0 to provide SRAM addresses.
DQ7-DQ0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Flash Erase/Program cycle. The outputs are in tri-state when OE#/BES# and BEF# are high.
BES#	SRAM Memory Bank Enable	To activate the SRAM memory bank when BES# is low. Note: BES# and OE# share pin 32. See Table 3 and 4 for the details of Operation Mode Selection.
BEF#	Flash Memory Bank Enable	To activate the Flash memory bank when BEF# is low.
OE#	Output Enable	To gate the data output buffers. Note: BES# and OE# share pin 32. See Table 3 and 4 for the details of Operation Mode Selection.
WE#	Write Enable	To control the Write operations.
VDD	Power Supply	To provide 3.0-3.6V supply
VSS	Ground	

Note: AMS = Most Significant Address

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**TABLE 3: FLASH OPERATION MODES SELECTION**

Mode	OE#	BEF#	WE#	A9	DQ	Address
Flash Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	A <sub>IN</sub>	D <sub>OUT</sub>	A <sub>IN</sub>
Flash Program	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	A <sub>IN</sub>	D <sub>IN</sub>	A <sub>IN</sub>
Flash Erase	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	X	X	Sector address, XXh for Bank-Erase
Standby	V <sub>IHC</sub>	V <sub>IHC</sub>	X	X	High Z	X
Flash Write Inhibit	V <sub>IL</sub>	X	X	X	High Z/D <sub>OUT</sub>	X
	X	X	V <sub>IH</sub>	X	High Z/D <sub>OUT</sub>	X
	X	V <sub>IH</sub>	X	X	High Z/D <sub>OUT</sub>	X
Product Identification	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>H</sub>	Manufacturer Code (BF)	A <sub>18</sub> - A <sub>1</sub> = V <sub>IL</sub> , A <sub>0</sub> = V <sub>IL</sub>
					Device Code (16 H) ID Code	A <sub>18</sub> - A <sub>1</sub> = V <sub>IL</sub> , A <sub>0</sub> = V <sub>IH</sub> See Table 4

**Note:** (1) BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#. During SRAM operation, pin 32 will function as BES#.

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**TABLE 4: SRAM OPERATION MODES SELECTION**

Mode	BES# <sup>(2)</sup>	BEF#	WE#	A9	DQ	Address
SRAM Read	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	A <sub>IN</sub>	D <sub>OUT</sub>	A <sub>IN</sub>
SRAM Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	A <sub>IN</sub>	D <sub>IN</sub>	A <sub>IN</sub>
Standby	V <sub>IHC</sub>	V <sub>IHC</sub>	X	X	High Z	X

**Note:** (2) BES# and OE# share pin 32. During flash operation, pin 32 functions as OE#. During SRAM operation, pin 32 will function as BES#.

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**TABLE 5: SOFTWARE COMMAND SEQUENCE FOR FLASH MEMORY BANK**

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr <sup>(1)</sup>	Data	Addr <sup>(1)</sup>	Data	Addr <sup>(1)</sup>	Data	Addr <sup>(1)</sup>	Data	Addr <sup>(1)</sup>	Data	Addr <sup>(1)</sup>	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA <sup>(3)</sup>	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA <sub>x</sub> <sup>(2)</sup>	30H
Bank-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry <sup>(6,7)</sup>	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

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**Notes:**

- (1) Address format A<sub>14</sub>-A<sub>0</sub> (Hex), Addresses A<sub>15</sub>, A<sub>16</sub>, A<sub>17</sub> and A<sub>18</sub> are a “Don’t Care” for the Command sequence.
- (2) SA<sub>x</sub> for Sector-Erase; uses A<sub>18</sub>-A<sub>12</sub> address lines
- (3) BA = Program Byte address
- (4) With A<sub>18</sub>-A<sub>1</sub>=0; SST Manufacturer Code = BFH, is read with A<sub>0</sub> = 0, 31LF041A Device Code = 16 H, is read with A<sub>0</sub> = 1.
- (5) The device does not remain in Software Product ID Mode if powered down.

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential .....	-0.5V to V <sub>DD</sub> + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential .....	-1.0V to V <sub>DD</sub> + 1.0V
Voltage on A <sub>9</sub> Pin to Ground Potential .....	-0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C) .....	1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) .....	240°C
Output Short Circuit Current <sup>(1)</sup> .....	50 mA

**Note:** <sup>(1)</sup> Outputs shorted for no more than one second. No more than one output shorted at a time.

**OPERATING RANGE**

Range	Ambient Temp	V <sub>DD</sub>
Commercial	0 °C to +70 °C	3.0-3.6V
Industrial	-40 °C to +85 °C	3.0-3.6V

**AC CONDITIONS OF TEST**

Input Rise/Fall Time .....	5 ns
Output Load .....	C <sub>L</sub> = 30 pF
See Figures 14 and 15	



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**TABLE 6: DC OPERATING CHARACTERISTICS  $V_{DD} = 3.0-3.6V$**

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I <sub>DD</sub>	Power Supply Current				$V_{DD} = V_{DD} \text{ Max}$ , all DQs open, Address input = $V_{IL}/V_{IH}$ , at $f=1/T_{RC} \text{ Min}$ . OE# = $V_{IL}$ , WE# = $V_{IH}$ BEF# = $V_{IL}$ , BES# = $V_{IH}$ BEF# = $V_{IH}$ , BES# = $V_{IL}$ BEF# = $V_{IH}$ , BES# = $V_{IL}$
	Read				
	Flash		12	mA	
	SRAM		40	mA	
	Concurrent Operation		55	mA	
	Write				OE# = $V_{IH}$ , WE# = $V_{IL}$
	Flash (Program)		15	mA	BEF# = $V_{IL}$ , BES# = $V_{IH}$
	SRAM		40	mA	BEF# = $V_{IH}$ , BES# = $V_{IL}$
I <sub>SB</sub> <sup>(1)</sup>	Standby $V_{DD}$ Current		30	$\mu A$	$V_{DD} = V_{DD} \text{ Max}$ . BEF# = BES# = $V_{IHC}$
I <sub>LI</sub>	Input Leakage Current		1	$\mu A$	$V_{IN} = GND$ to $V_{DD}$ , $V_{DD} = V_{DD} \text{ Max}$ .
I <sub>LO</sub>	Output Leakage Current		1	$\mu A$	$V_{OUT} = GND$ to $V_{DD}$ , $V_{DD} = V_{DD} \text{ Max}$ .
V <sub>IL</sub>	Input Low Voltage		0.4	V	$V_{DD} = V_{DD} \text{ Min}$ .
V <sub>IH</sub>	Input High Voltage	0.7 $V_{DD}$		V	$V_{DD} = V_{DD} \text{ Max}$ .
V <sub>IHC</sub>	Input High Voltage (CMOS)	$V_{DD}-0.3$		V	$V_{DD} = V_{DD} \text{ Max}$ .
V <sub>OL</sub>	Output Low Voltage		0.2	V	$I_{OL} = 100 \mu A$ , $V_{DD} = V_{DD} \text{ Min}$ .
V <sub>OH</sub>	Output High Voltage	$V_{DD}-0.2$		V	$I_{OH} = -100 \mu A$ , $V_{DD} = V_{DD} \text{ Min}$ .
V <sub>H</sub>	Supervoltage for A <sub>9</sub> pin	11.4	12.6	V	BEF# = OE# = $V_{IL}$ , WE# = $V_{IH}$
I <sub>H</sub>	Supervoltage Current		200	$\mu A$	BEF# = OE# = $V_{IL}$ , WE# = $V_{IH}$ , A <sub>9</sub> = $V_H$ Max. for A <sub>9</sub> pin

**Note:** <sup>(1)</sup>Specification applies to commercial devices only. This parameter may be higher for industrial devices.

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**TABLE 7: RECOMMENDED SYSTEM POWER-UP TIMINGS**

Symbol	Parameter	Minimum	Units
T <sub>PU-READ</sub> <sup>(2)</sup>	Power-up to Read Operation	100	$\mu s$
T <sub>PU-WRITE</sub> <sup>(2)</sup>	Power-up to Write Operation	100	$\mu s$

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**Note:** <sup>(2)</sup>This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 8: CAPACITANCE ( $T_a = 25^\circ C$ ,  $f=1 \text{ Mhz}$ , other pins open)**

Parameter	Description	Test Condition	Maximum
C <sub>I/O</sub> <sup>(2)</sup>	I/O Pin Capacitance	$V_{I/O} = 0V$	12 pF
C <sub>IN</sub> <sup>(2)</sup>	Input Capacitance	$V_{IN} = 0V$	6 pF

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**Note:** <sup>(2)</sup>This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



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**TABLE 9: RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Minimum Specification	Units	Test Method
N <sub>END</sub> <sup>(1)</sup>	Endurance	10,000	Cycles	JEDEC Standard A117
T <sub>DR</sub> <sup>(1)</sup>	Data Retention	100	Years	JEDEC Standard A103
V <sub>ZAP_HBM</sub> <sup>(1)</sup>	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V <sub>ZAP_MM</sub> <sup>(1)</sup>	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I <sub>LTH</sub> <sup>(1)</sup>	Latch Up	100 + I <sub>DD</sub>	mA	JEDEC Standard 78

**Note:** <sup>(1)</sup>This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

382PGMT9.0

**TABLE 10: SRAM READ CYCLE TIMING PARAMETERS V<sub>DD</sub> = 3.0-3.6V**

Symbol	Parameter	Min	Max	Unit
T <sub>RCS</sub>	Read Cycle Time	300		ns
T <sub>AAS</sub>	Address Access Time		300	ns
T <sub>BES</sub>	Bank Enable Access Time		300	ns
T <sub>BLZS</sub> <sup>(1)</sup>	BES# to Active Output	15		ns
T <sub>BHZS</sub> <sup>(1)</sup>	BES# to High-Z Output		30	ns
T <sub>OHS</sub> <sup>(1)</sup>	Output Disable to High-Z Output		30	ns
T <sub>OHS</sub>	Output Hold from Address Change	10		ns

**Note:** <sup>(1)</sup> This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

382PGMT10.2

**TABLE 11: SRAM WRITE CYCLE TIMING PARAMETERS V<sub>DD</sub> = 3.0-3.6V**

Symbol	Parameter	Min	Max	Unit
T <sub>WCS</sub>	Write Cycle Time	300		ns
T <sub>BWS</sub>	Bank Enable to End-of-Write	230		ns
T <sub>AWS</sub>	Address Valid to End-of-Write	230		ns
T <sub>ASTS</sub>	Address Set-up Time	0		ns
T <sub>WPS</sub>	Write Pulse Width	200		ns
T <sub>WRS</sub>	Write recovery Time	0		ns
T <sub>DSS</sub>	Data Set-up Time	150		ns
T <sub>DHS</sub>	Data Hold from Write Time	0		ns

382PGMT11.2



AC CHARACTERISTICS

TABLE 12: FLASH READ CYCLE TIMING PARAMETERS  $V_{DD} = 3.0-3.6V$

Symbol	Parameter	Min	Max	Units
$T_{RC}$	Read Cycle Time	300		ns
$T_{BE}$	Bank Enable Access Time		300	ns
$T_{AA}$	Address Access Time		300	ns
$T_{OE}$	Output Enable Access Time		150	ns
$T_{BLZ}^{(1)}$	BEF# Low to Active Output	0		ns
$T_{OLZ}^{(1)}$	OE# Low to Active Output	0		ns
$T_{BHZ}^{(1)}$	BEF# High to High-Z Output		60	ns
$T_{OHZ}^{(1)}$	OE# High to High-Z Output		60	ns
$T_{OH}^{(1)}$	Output Hold from Address Change	0		ns

Note: <sup>(1)</sup>This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

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TABLE 13: FLASH PROGRAM/ERASE CYCLE TIMING PARAMETERS  $V_{DD} = 3.0-3.6V$

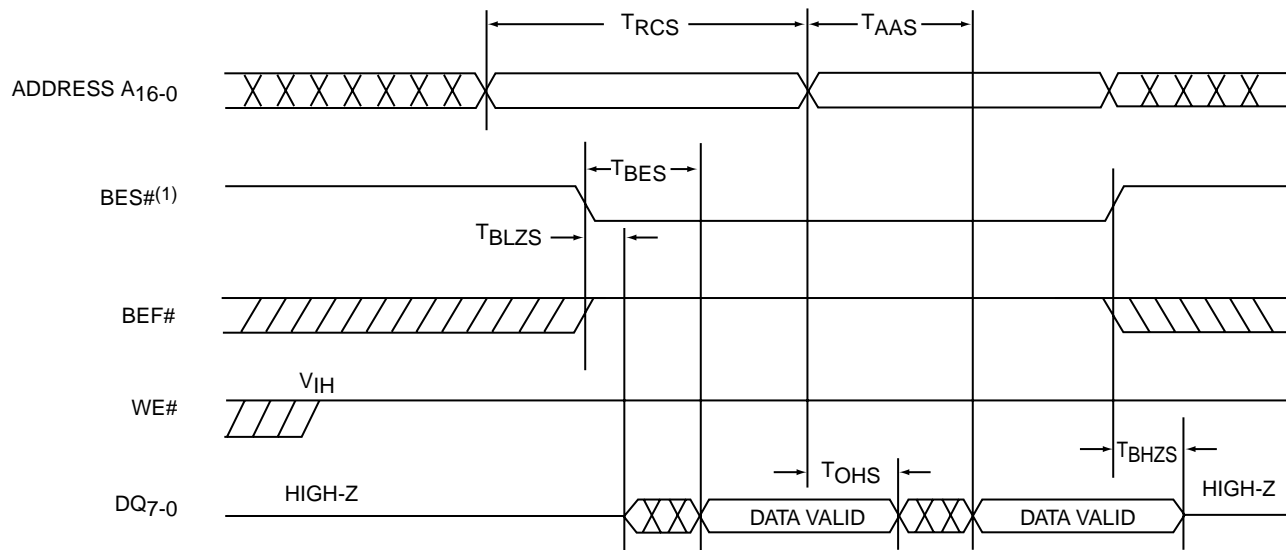
Symbol	Parameter	Min	Max	Units
$T_{BP}$	Byte-Program Time		20	$\mu s$
$T_{AS}$	Address Setup Time	0		ns
$T_{AH}$	Address Hold Time	50		ns
$T_{BS}$	WE# and BEF# Setup Time	0		ns
$T_{BH}$	WE# and BEF# Hold Time	0		ns
$T_{OES}$	OE# High Setup Time	0		ns
$T_{OEH}$	OE# High Hold Time	10		ns
$T_{BP}$	BEF# Pulse Width	100		ns
$T_{WP}$	WE# Pulse Width	100		ns
$T_{WPH}$	WE# Pulse Width High	50		ns
$T_{BPH}$	BEF# Pulse Width High	50		ns
$T_{DS}$	Data Setup Time	50		ns
$T_{DH}$	Data Hold Time	0		ns
$T_{IDA}$	Software ID Access and Exit Time		150	ns
$T_{SE}$	Sector-Erase		25	ms
$T_{SBE}$	Bank-Erase		100	ms
$T_{BS}$	Bank Enable Setup time for Concurrent Operation	0		ns

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# 4 Megabit Flash + 1 Megabit SRAM ComboMemory SST31LF041A

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Note 1: BES# and OE# share pin 32. During SRAM operation, pin 32 functions as BES#.

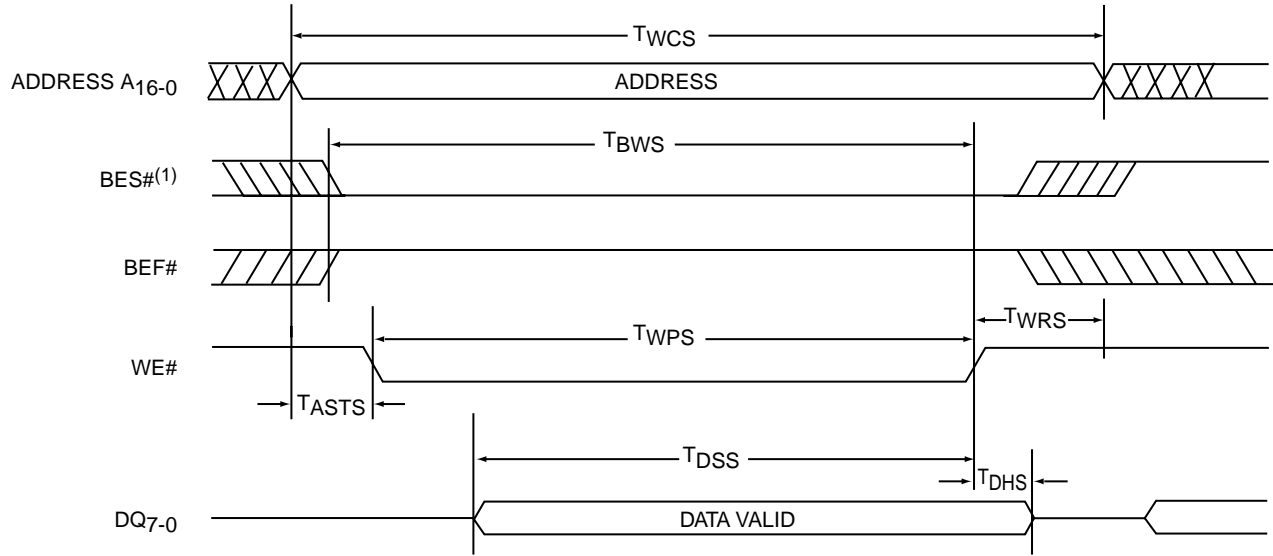
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FIGURE 2: SRAM READ CYCLE TIMING DIAGRAM



# 4 Megabit Flash + 1 Megabit SRAM ComboMemory SST31LF041A

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Note 1: BES# and OE# share pin 32. During SRAM operation, pin 32 functions as BES#.

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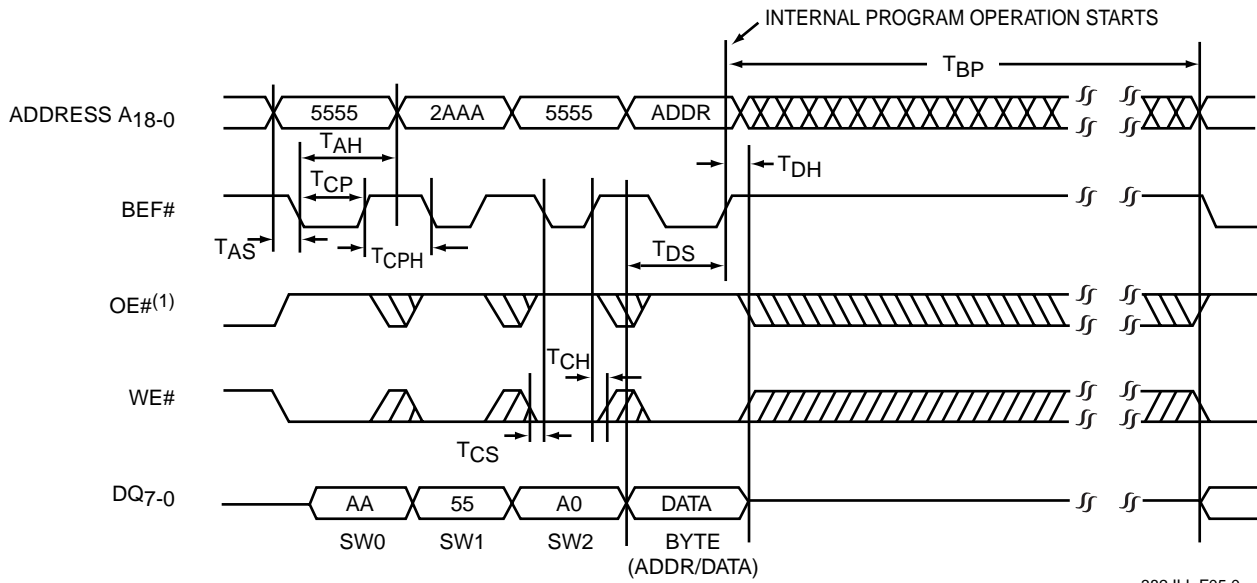
FIGURE 3: SRAM WRITE CYCLE TIMING DIAGRAM





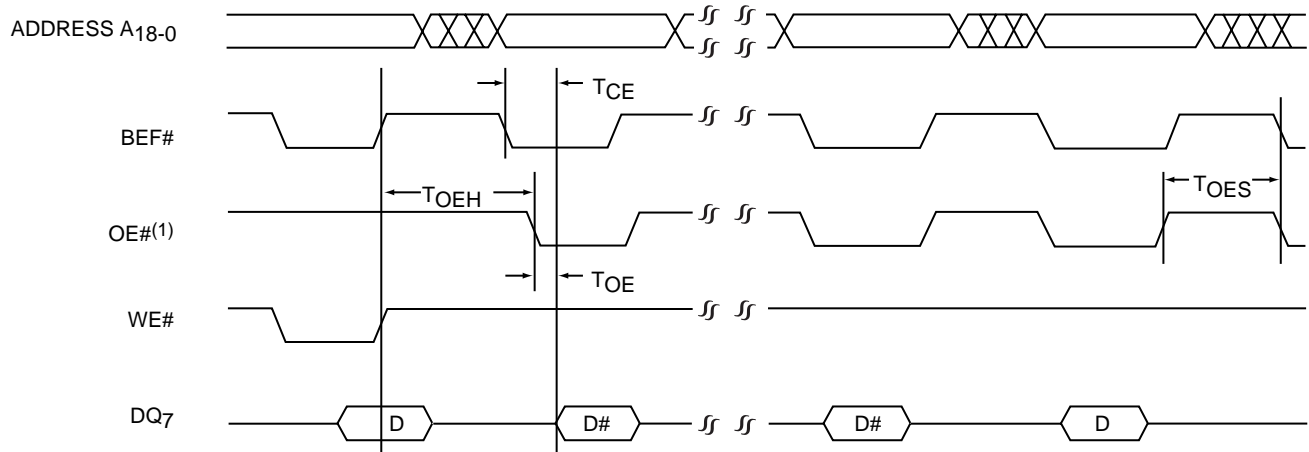
# 4 Megabit Flash + 1 Megabit SRAM ComboMemory SST31LF041A

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Note 1: BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 6: FLASH BEF# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



Note 1: BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 7: FLASH DATA# POLLING TIMING DIAGRAM



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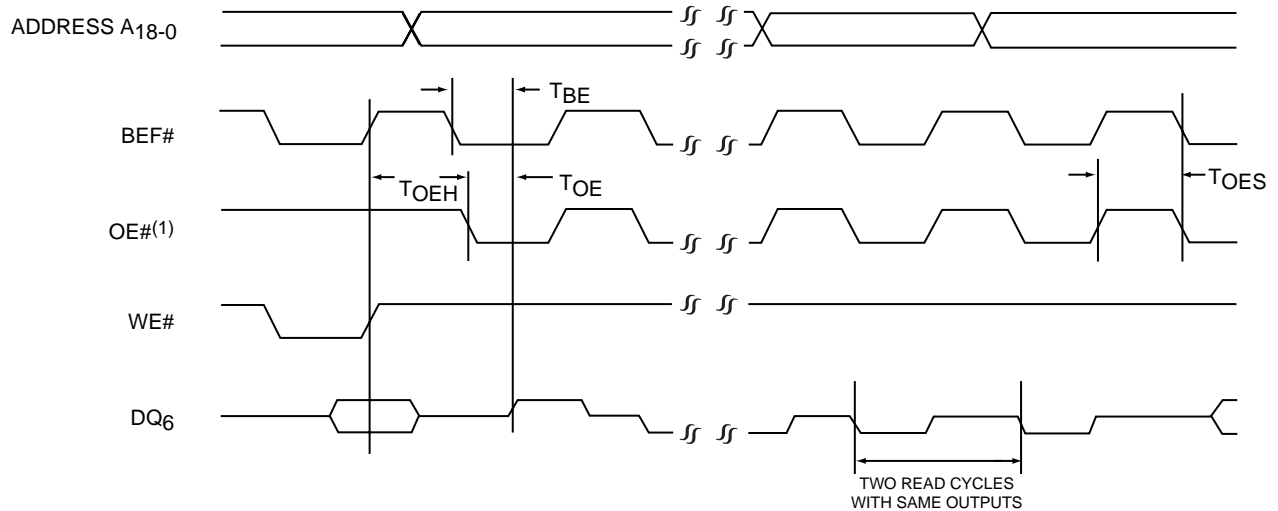


FIGURE 8: FLASH TOGGLE BIT TIMING DIAGRAM

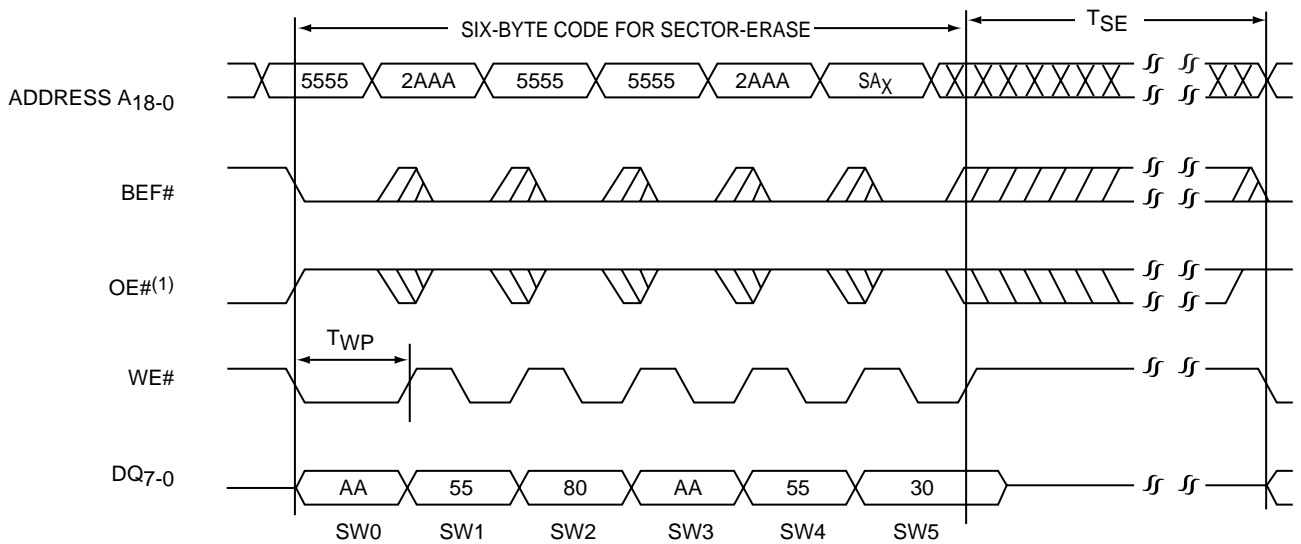
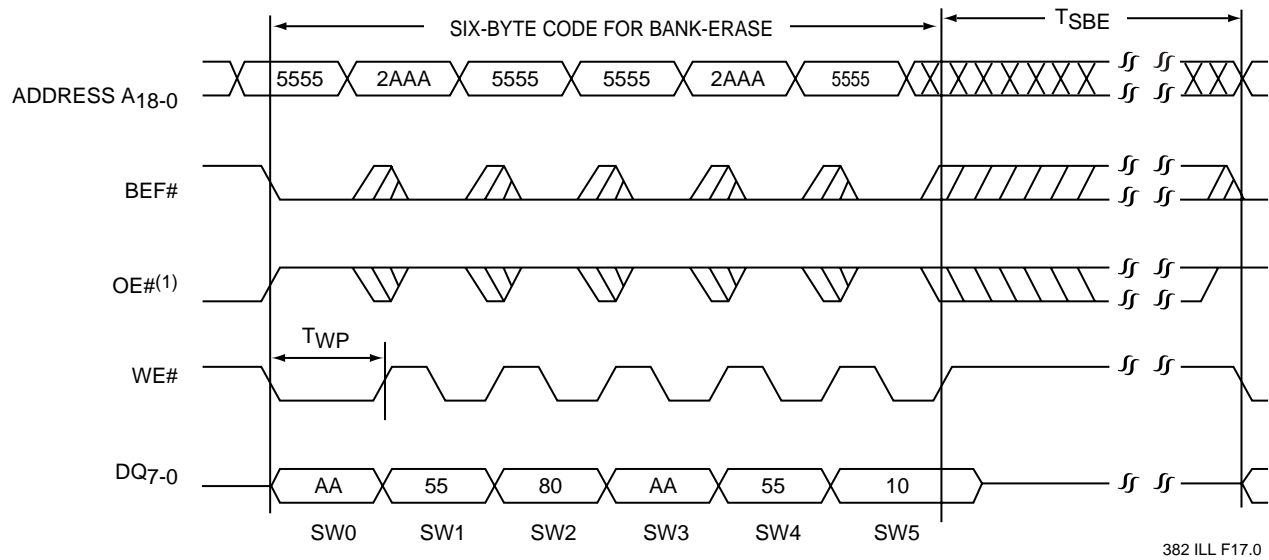


FIGURE 9: FLASH WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM



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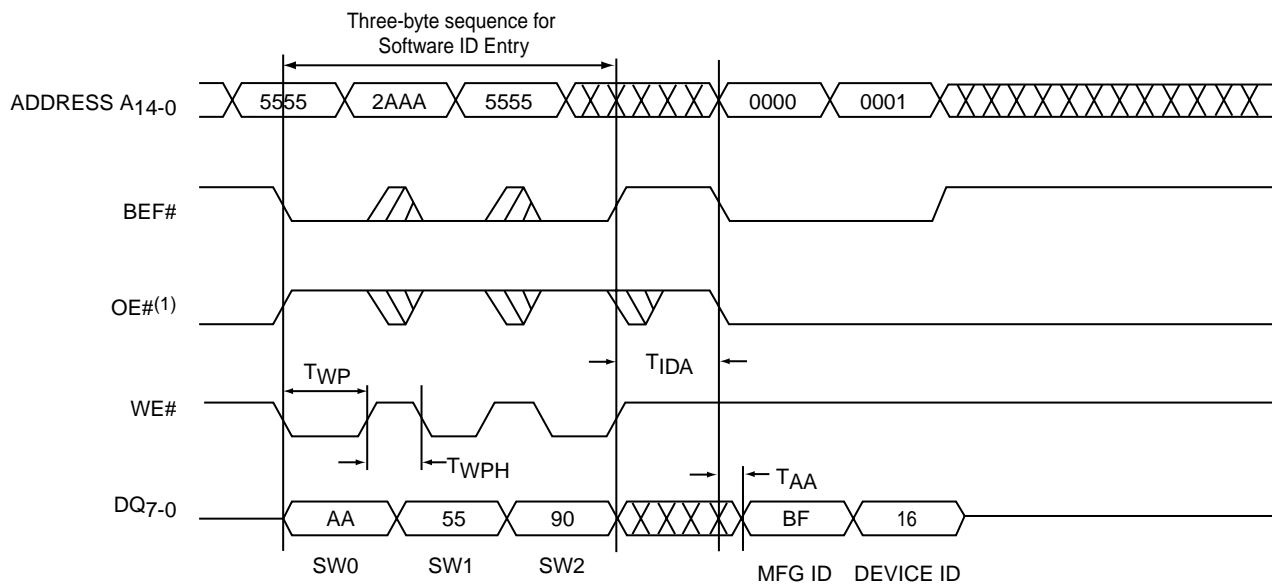
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Note: The device also supports BEF# controlled Bank-Erase operation. The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See table 10)

Note 1: BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

**FIGURE 10: FLASH WE# CONTROLLED BANK-ERASE TIMING DIAGRAM**



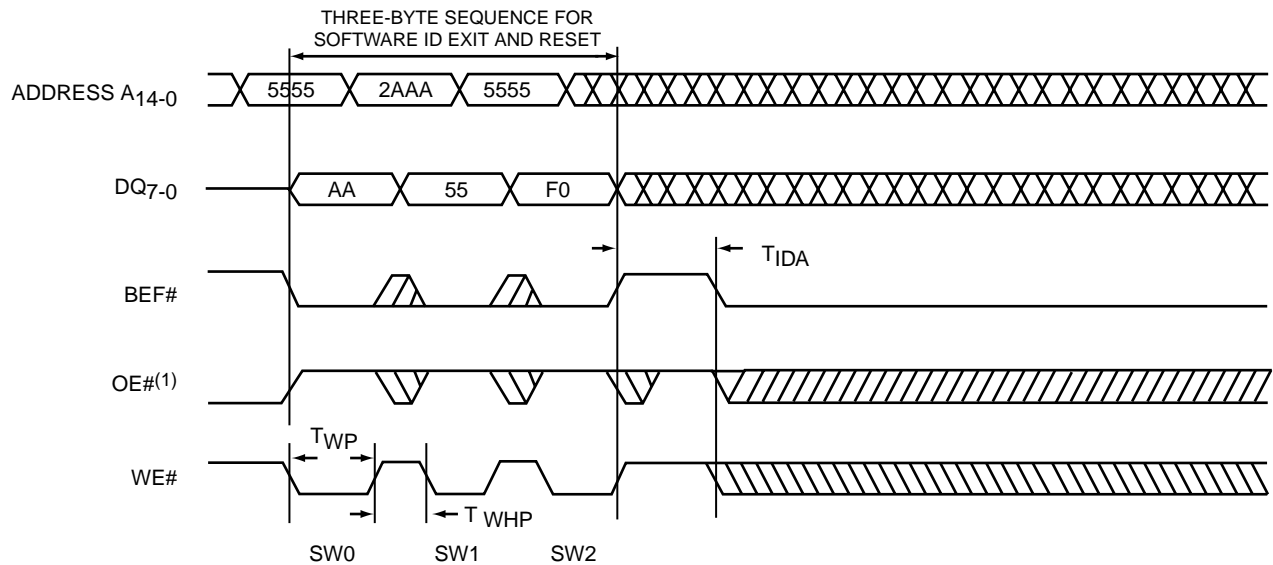
Note 1: BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

**FIGURE 11: FLASH SOFTWARE ID ENTRY AND READ**



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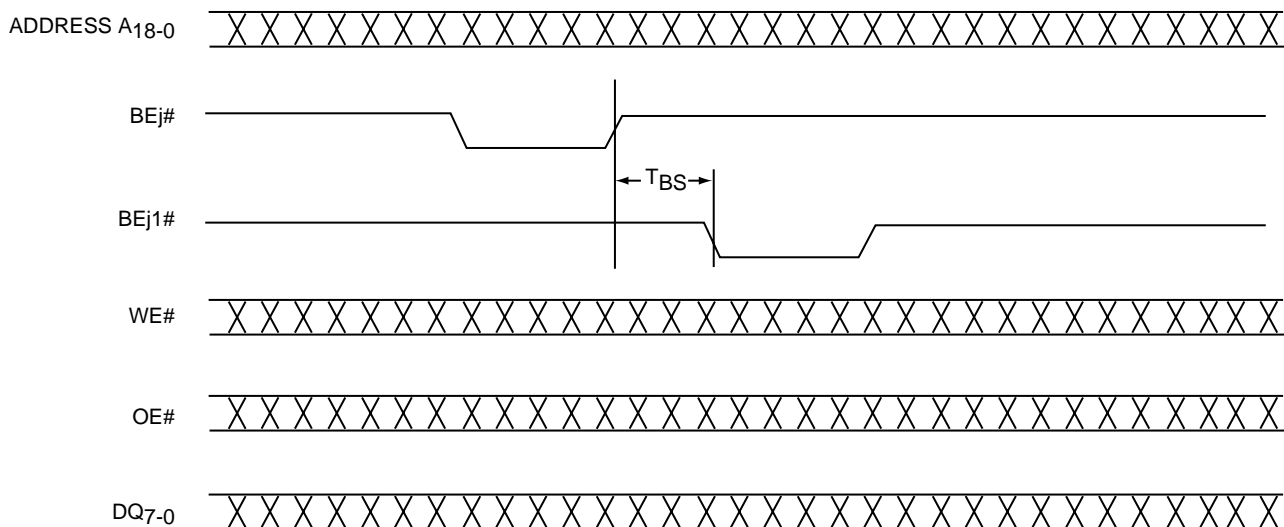
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Note 1: BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

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FIGURE 12: FLASH SOFTWARE ID EXIT AND RESET



Note: j = F or S  
j1 = S or F

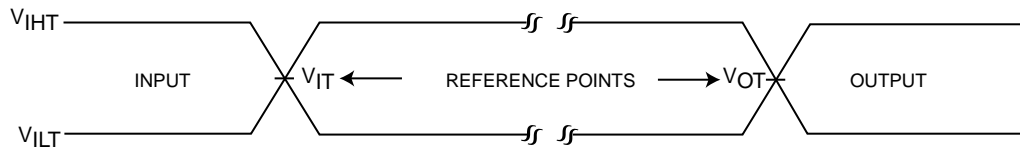
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FIGURE 13: TIMING DIAGRAM FOR ALTERNATING BETWEEN FLASH/SRAM TO SRAM/FLASH



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AC test inputs are driven at  $V_{IHT}$  ( $0.9 V_{DD}$ ) for a logic "1" and  $V_{ILT}$  ( $0.1 V_{DD}$ ) for a logic "0".  
Measurement reference points for inputs and outputs are at  $V_{IT}$  ( $0.5 V_{DD}$ ) and  $V_{OT}$  ( $0.5 V_{DD}$ )  
Input rise and fall times (10%  $\leftrightarrow$  90%) are  $<5$  ns.

Output level per common SRAM test standards.

FIGURE 14: AC INPUT/OUTPUT REFERENCE WAVEFORMS

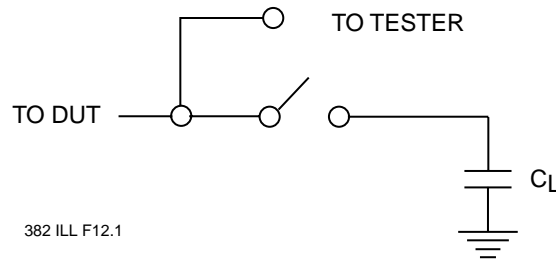


FIGURE 15: A TEST LOAD EXAMPLE



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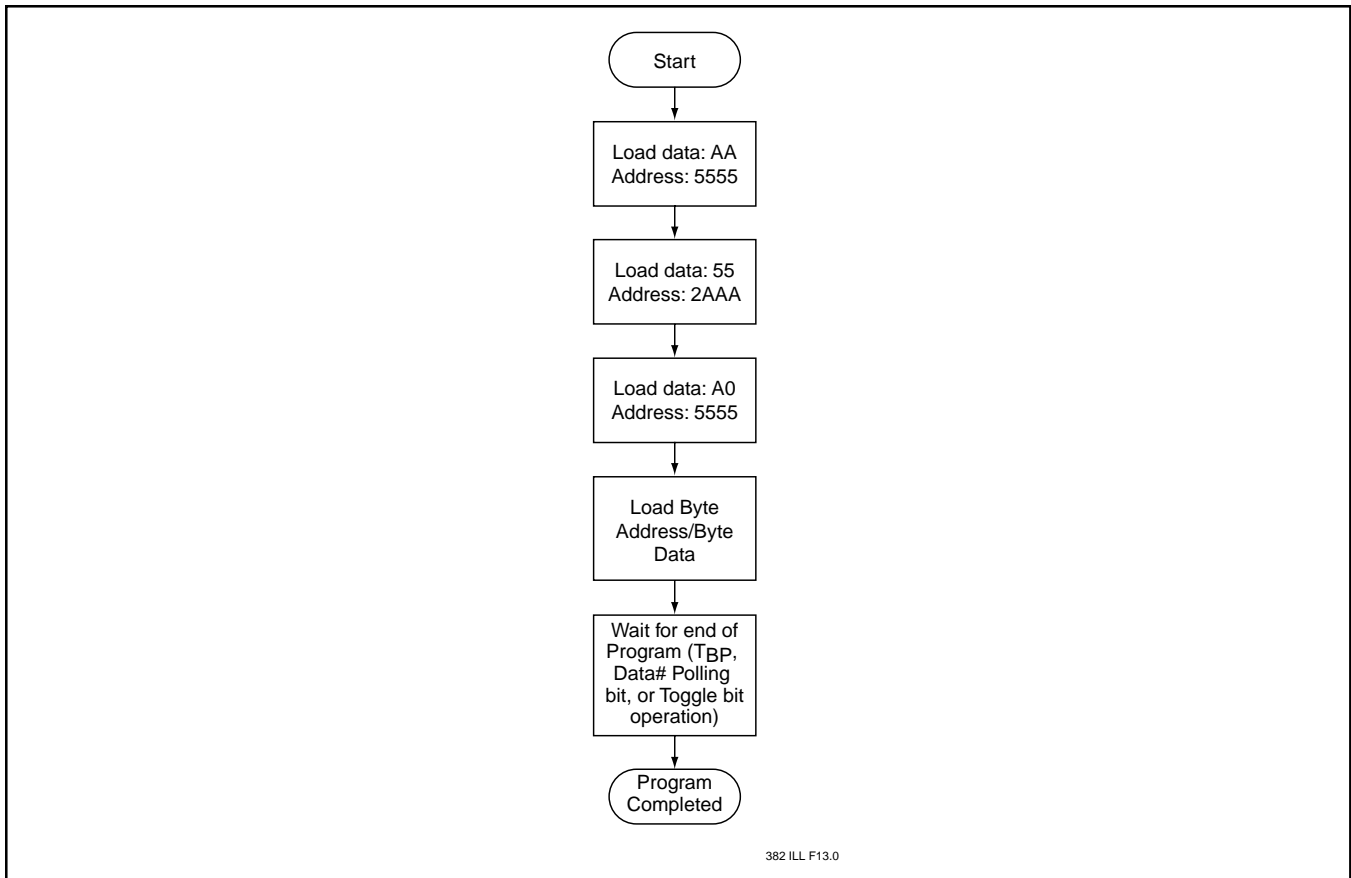


FIGURE 16: BYTE-PROGRAM ALGORITHM

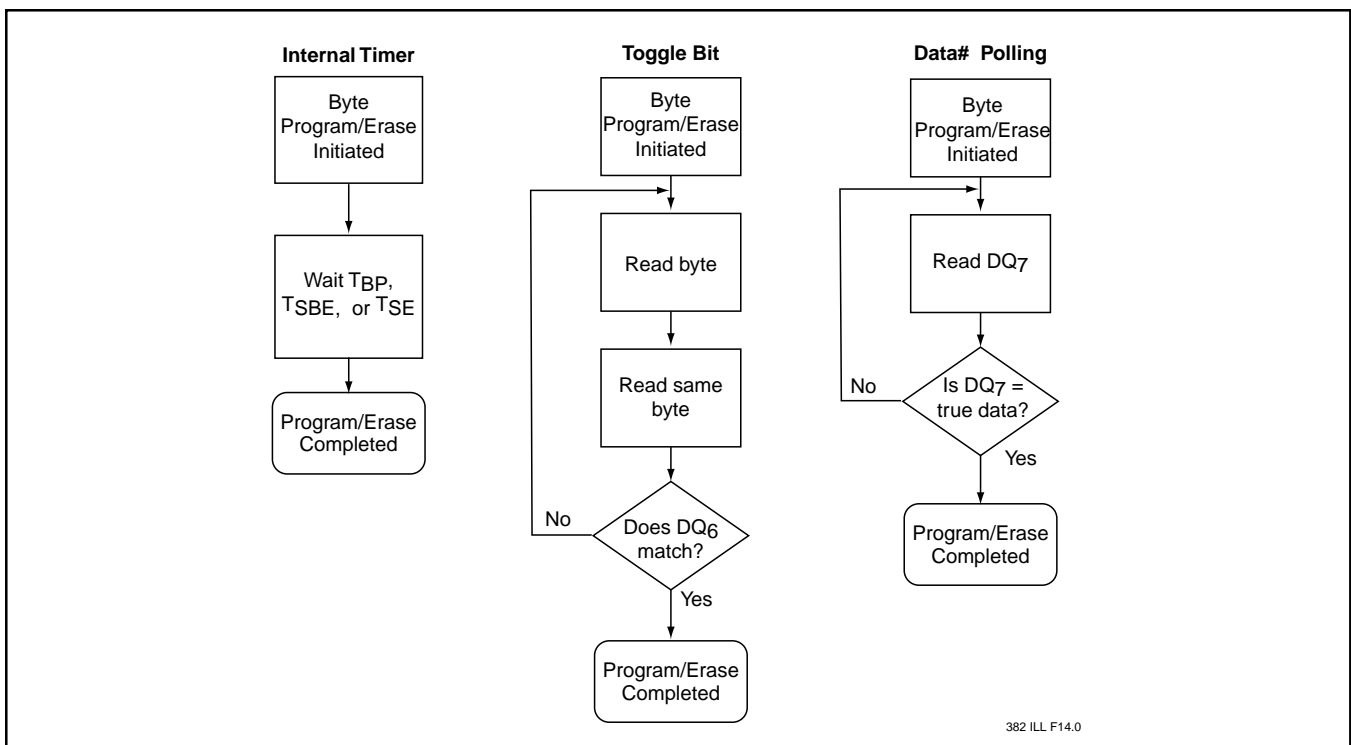
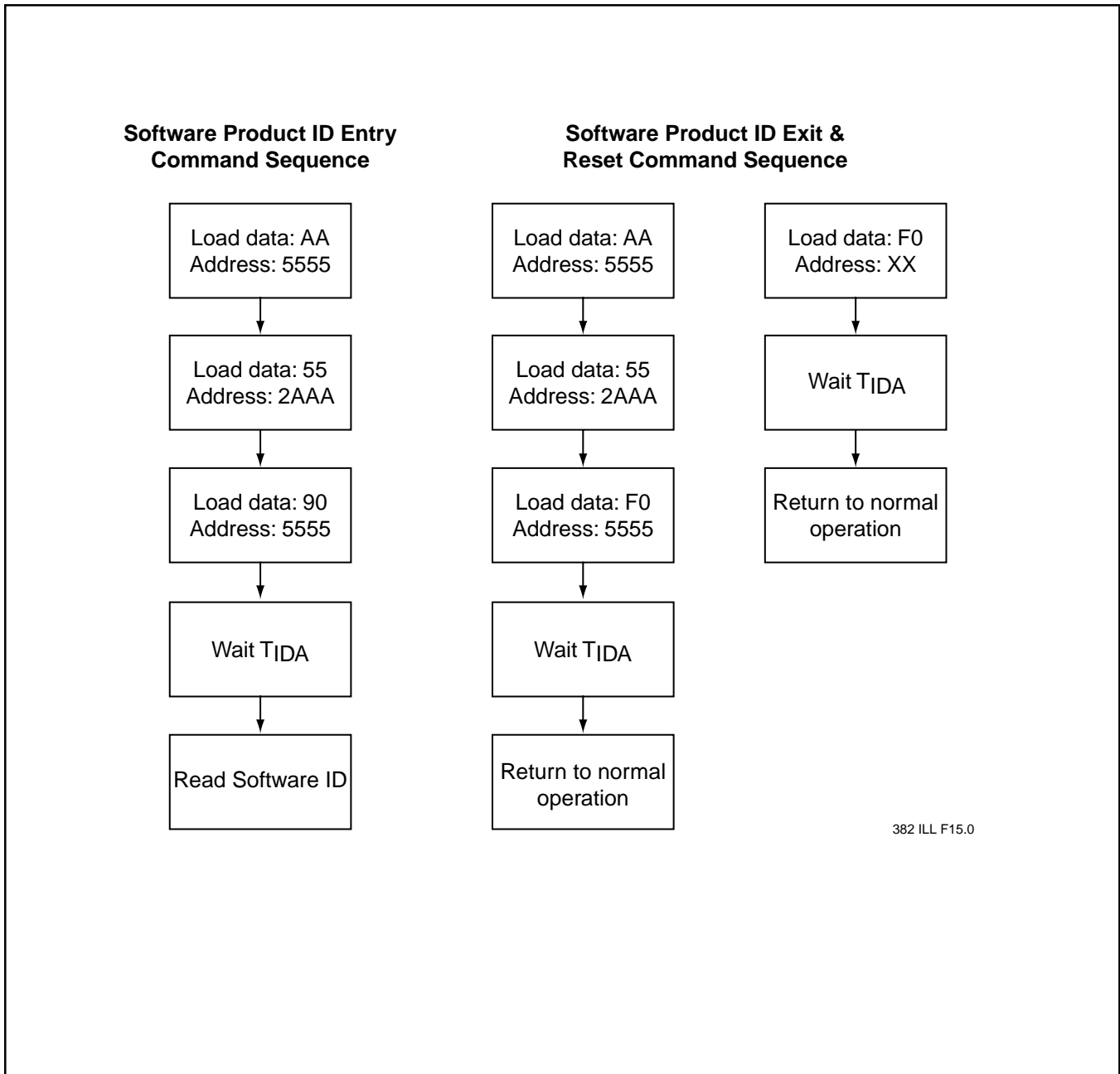


FIGURE 17: WAIT OPTIONS



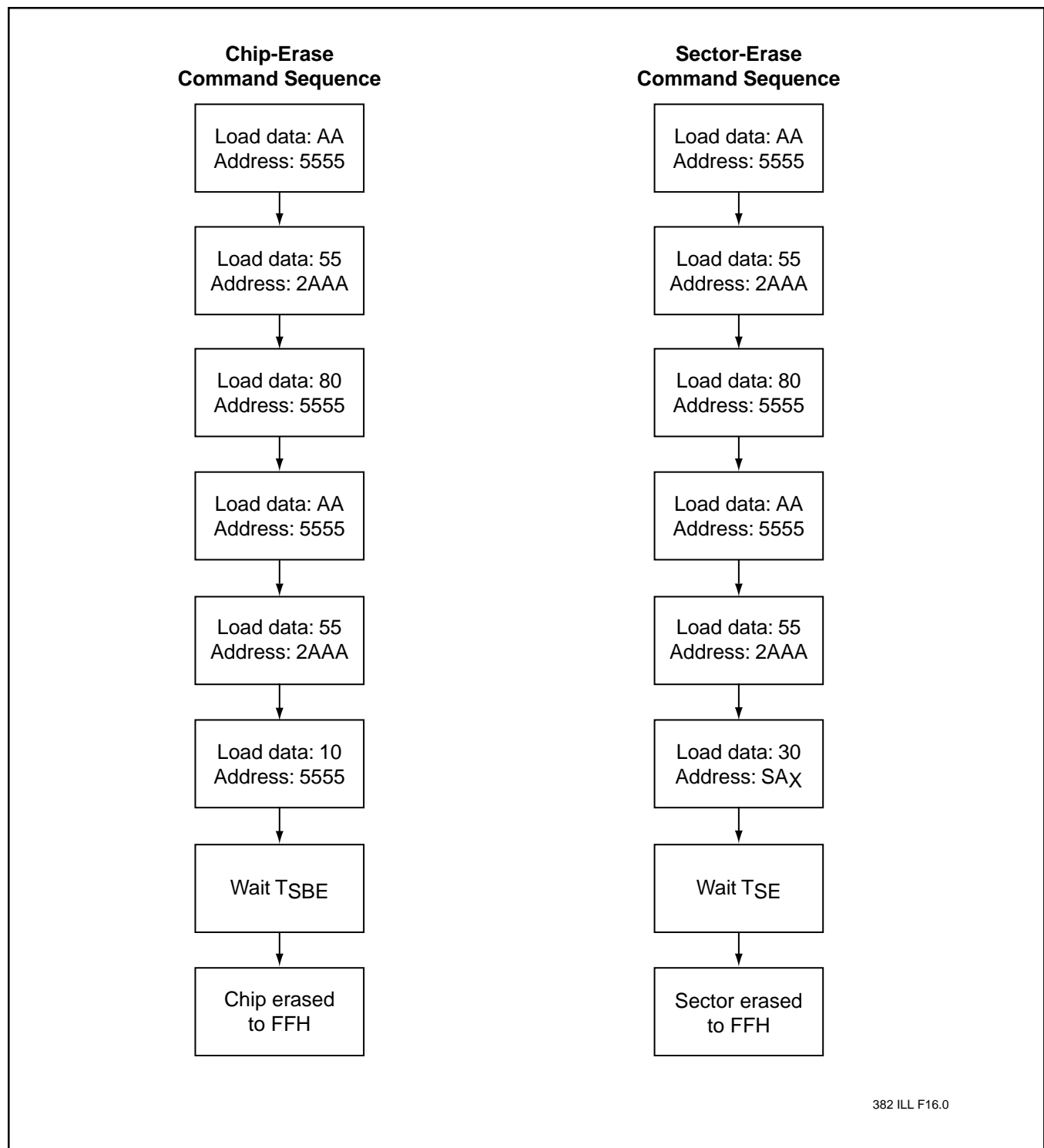
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FIGURE 18: SOFTWARE PRODUCT COMMAND FLOWCHARTS



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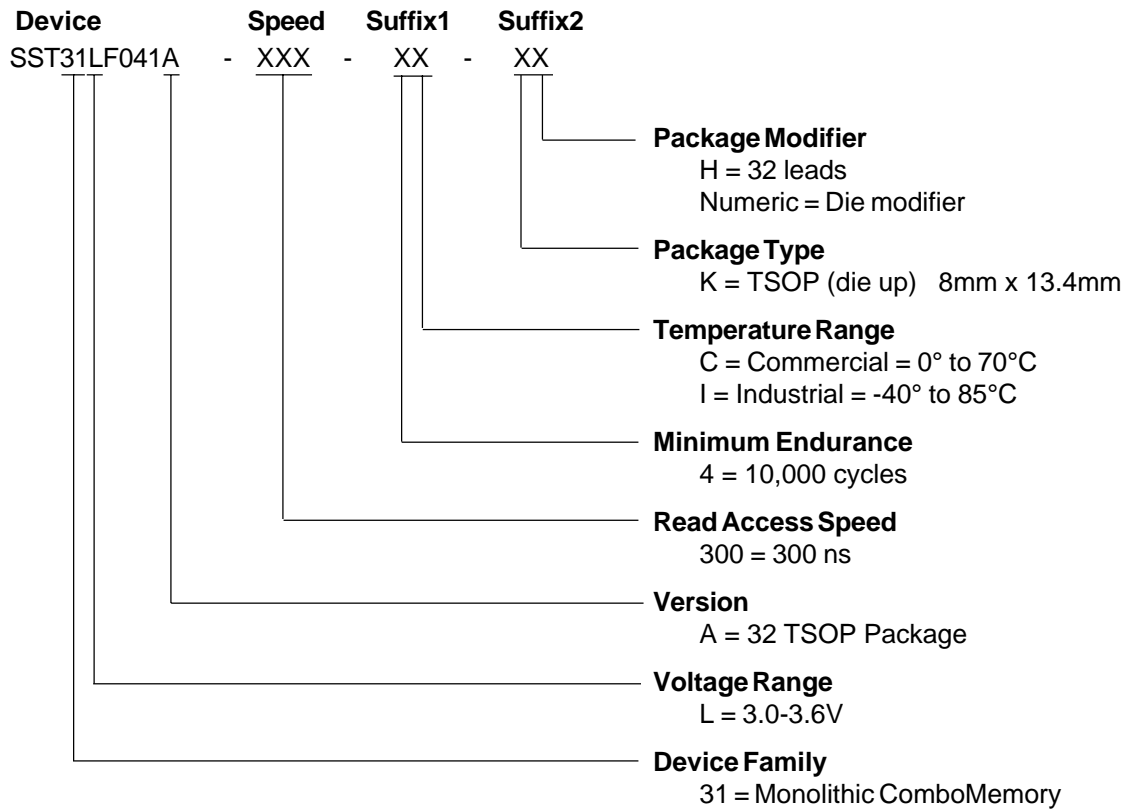
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FIGURE 19: ERASE COMMAND SEQUENCE



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### SST31LF041A Valid combinations

SST31LF041A-300-4C-KH

SST31LF041A-300-4I-KH

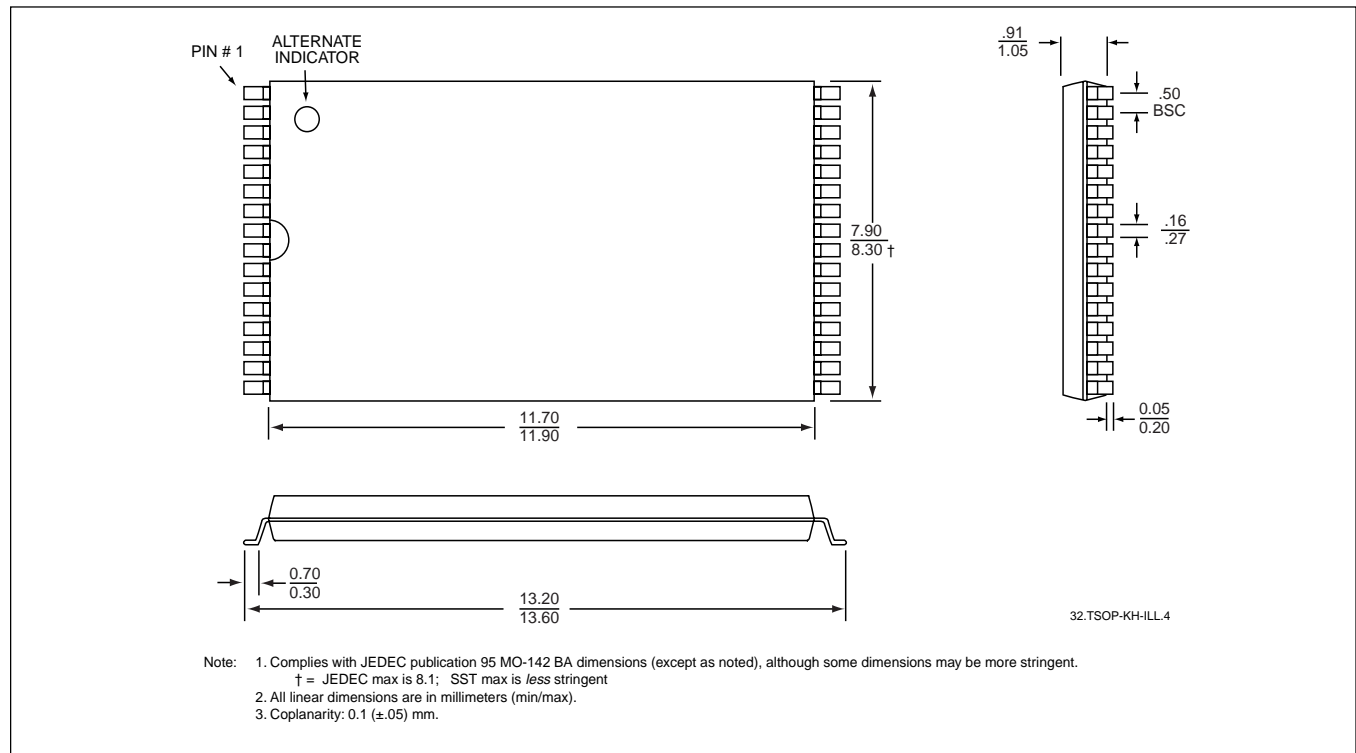
**Example:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



# 4 Megabit Flash + 1 Megabit SRAM ComboMemory SST31LF041A

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## PACKAGING DIAGRAMS



**32-PIN THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 13.4MM**  
**SST PACKAGE CODE: KH**



**4 Megabit Flash + 1 Megabit SRAM ComboMemory  
SST31LF041A**

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