Implement 3.3Vdual using AIC1730 for DRAM Supply on IAPC Motherboard

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Introduction

Today, PCs need to remain constantly connected to the outside world, but at the same time consume minimum power. Even looking “idle”, it is still possible to receive a message from the Internet, an incoming fax, or a phone call. The PC must wake up from “sleep” mode to “on” mode automatically, that is, to be an Instantly Available PC (IAPC)

The “Advanced Configuration and Power Interface”, or ACPI, is a system for controlling the use of power in a computer. It enables the computer manufacturer and the computer user to determine the computer power usage dynamically.

As the ACPI specified, there are 3 ACPI states that are of primary concerns to the system designer, designated S0, S3 and S5. S0 is the full-power state, the state of the computer when it is being actively used. The other two states are sleep states, reflecting differing levels of power-down.

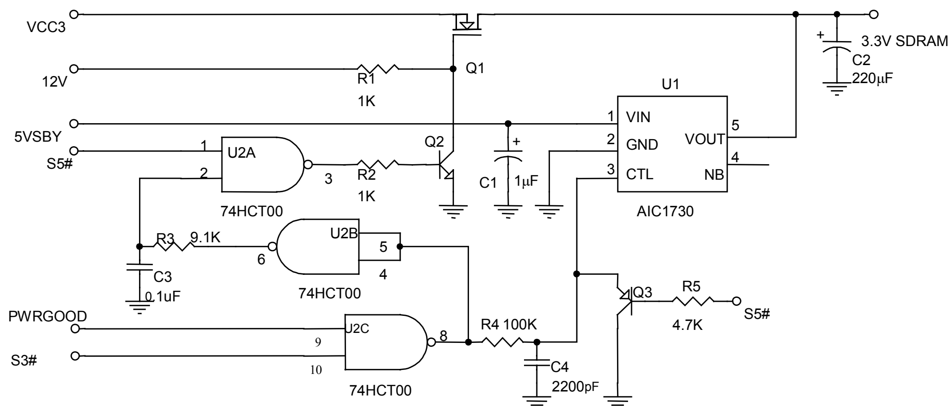
S3 and S5

S3 is a state in which the processor is powered down, but its last state is reserved in IC memory, which is kept on. Since access speed of memory is fast, the computer can quickly come back up to full operation. However, this state continues to draw moderate power, due to the memory, which has been kept alive and also called STR (Suspend to RAM).

S5 is a state in which memory is off, and the last state of the processor has been written to the hard disk. Since the access time of disk is slow, the computer takes longer time to come back to full operation. However, since memory is off, this state draws minimal power.

Operation Description

The 3.3V SDRAM output is intended to provide power to SDRAM memory. Most system will use this power. The 3.3V SDRAM is generated by either one of the two sources, which are +3.3V main and linear regulator from +5V standby, as shown in Figure 1. When main power is present, the MOSFET Q1 is turned on as a switch. That makes input and output connected. When the main power is absent, the linear regulator is activated and generating a regulated 3 3V from +5V standby. The MOSFET Q1 must be connected as shown in the figure to avoid back-feed.



Note:Remove Q3 and R5 and connect pin 1 and Pin 2 of U2A together, if 3.3V is not supplied at Soft-off.

Fig.1 AIC1730 IAPC 3.3V SDRAM for MB solution

The state of the external switch (MOSFET) and LDO are controlled by the S3#, S5# and PWRGOOD (PWR_OK) lines. When S5# is de-asserted, both the external switch and LDO are off, and no output voltage on 3.3V SDRAM line.

Once if the S5# line is asserted, the 3.3V SDRAM output is on. In this condition, no matter S3# or the PWRGOOD signal, or both, are de-asserted, the LDO is on and the external switch is off. Only in the case of both the S3# and the PWRGOOD signal are asserted, the external switch is on and LDO is off.

In a typical system, it is expected that standby current will be about 150mA maximum. Full operating current will be as high as 4.8A maximum, so that external switch must have a low RDSON in order to prevent unacceptable voltage dropout. Figure 2 below illustrate a simplified block diagram with the truth table in table 1

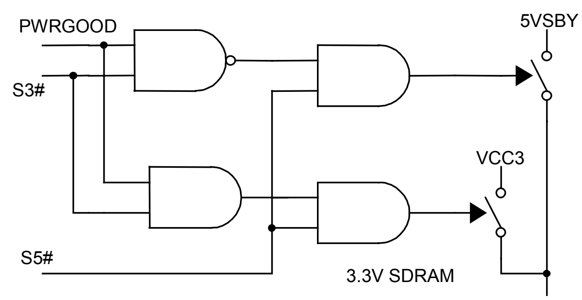


Fig. 2

S5#	PWRGOOD	S3#	3.3V SDRAM from
0	0	0	x
0	0	1	x
0	1	0	x
0	1	1	x
1	0	0	$5V_{SBY}$
1	0	1	$5V_{SBY}$
1	1	0	$5V_{SBY}$
1	1	1	V_{CC3}

Table 1. The 3.3Vdual output truth table

Application Information

AIC1730 overview

The AIC1730 implemented here is a 150mA LDO, which is originally used in some portable devices such as cellphone, PDA and pager etc… due to its shutdown function, ultra-low dropout, low noise and tiny little package.

Now it's implemented as an LDO, which can be shut down by the control logic in the application of motherboard for SDRAM power distribution.

Control logic

The control logic is designed not only to select the power route but also to minimize the output capacitance required to hold up the voltage dropout during transitions among different sleeping states. Thus, the 3.3V SDRAM output has guaranteed a 700uS delay time to cause the overlap times, the time during a state transition duration which both VCC3 and 5VSBY are connected to the output. This overlap time ensures that a power source is always connected to the output, so that there will be no dig in the output voltage during state transitions.

ATX power timing

Further, according to ATX specification revision 2.03, there are still various regulations specified to regulate the quality and electrical characteristics of the ATX SPS, and the time of PS_ON, PWR_OK, and germane voltage rails should be as following figure 3 with the description in table 2:

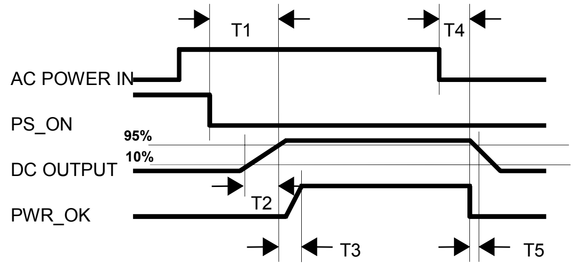


Fig.3 ATX power timing

Time	Description	Typical value
T1	Power on time	＜500ms
T2	Rise time	0.1ms＜T2＜20ms
T3	Power OK delay	100ms＜T3＜500ms
T4	AC loss to PWR_OK hold-up time	T4＞16 ms
T5	Power-down warning	T5＞1ms

Table 2. The ATX Rev.2.03 timing description table

In figure 3, the T3 is a time that PWR-OK was asserted after a time which the 3.3V、5V and 12V beyond the under voltage threshold (usually 95%). The T5 is a time, which PWR_OK was de-asserted before 3.3V, 5V and 12V, which fall below its under voltage threshold.

The power OK delay should be less than 500ms and power OK hold-up time should be more than 16ms for all of the SPS power. Basically, those are the most important parameter for 3.3V SDRAM output switched between 2 sources.

Combining the ATX regulations and the application of us, we get the clearly simplified diagrams as the following figures:

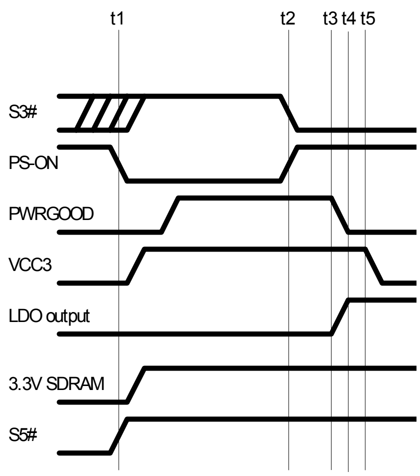


Fig.4 Timing diagram for S5 to S0 to S3

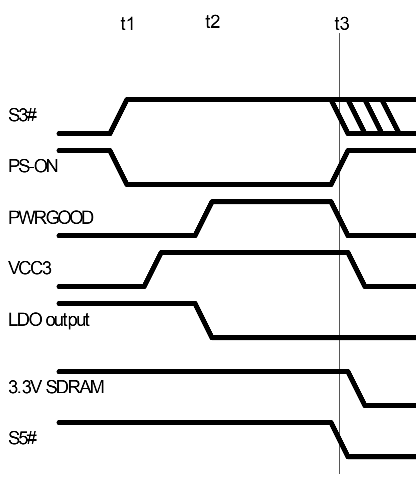


Fig.5 Timing diagram for S3 to S0 to S5

Transitions

Figure 4 shows the system in soft-off (S5) mode. 3.3V SDRAM output line should be low since VCC3 and LDO output are absent. Once the system activated at t1, the PS_ON asserted and 3.3V SDRAM output is eventually present, that is, the system is in full running mode (S0). The system didn't transit to S3 (Suspend To DRAM) until t2. The PWRGOOD line failed after a while. And according to the regulation, VCC3 is still valid for at least 1ms. Thus, it caused an overlap time that the 3.3V SDRAM connects to both power sources (i.e. t4 to t5).

The figure 5 shows the power supply becomes activated again with the waking up of the system from the S3 state to S0. Instead of LDO output, the 3.3V SDRAM now sources supply from VCC3 line, and the system transits into soft-off (S5) again after time t3. Now since SDRAM is no longer needed to maintain the content inside, the transition issue is not so important here. Further, the transition issue from S5 to S0 in figure 4 is no need to be cared as well.

Transient characteristics

An active load is used, setting the load current of 50mA and 150mA respectively at 3.3V. The transient characteristics are shown below:

CH1: S3#、2V/100ms

CH2: 3.3V SDRAM、500mV/100ms

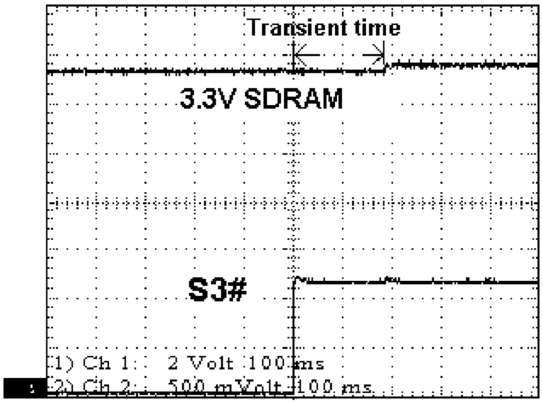


Fig.6 S3 to S0

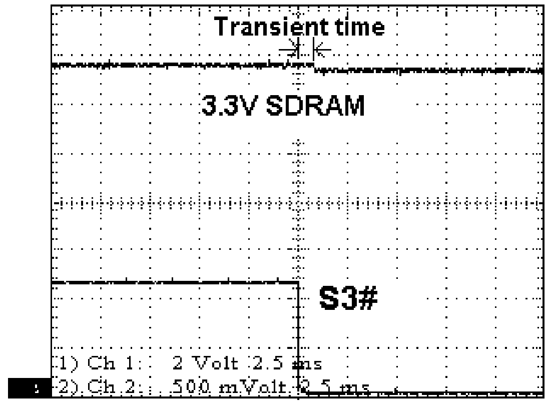


Fig.7 S0 to S3

Figure 6 shows the output current is 50mA. And 3.3V SDRAM switched from AIC1730 LDO output to VCC3 at the time when S3# line was de-asserted. There is no dig coming with the output line. Figure 7 also shows the output current is 50mA. And an overlap of both two input sources is caused by a 700us RC delay (R3、R4).

The following 2 figures show the transient when 150mA output current consumption on 3.3V SDRAM line, from both S3 to S0 and S0 to S3.

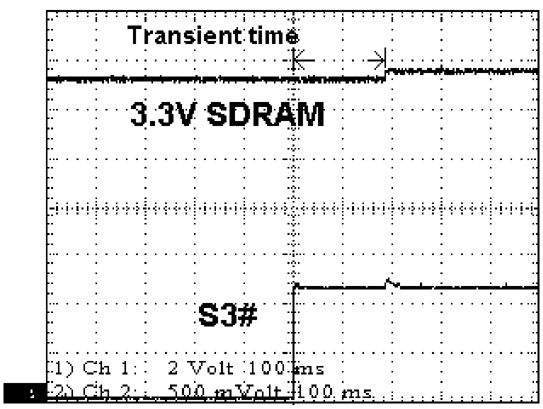


Fig.8 S3 to S0

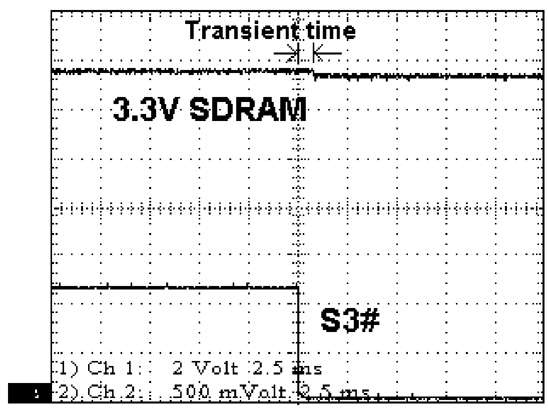


Fig.9 S0 to S3

Component Selection

Transistor Selection

Since the Q1 MOSFET serves as a switch during active state (S0), it should be sized based on load regulation requirement and the power consumption. A MOSFET with a low R_{DSON} and an acceptable package for power dissipation is recommended.

The maximum RDSON can be expressed as the following equation:

$$R_{DSON(MAX)} = \frac{V_{INMIN} - V_{OUTMIN}}{I_{OUTMAX}}$$

And it would be up to scratch for both Q2 and Q3. They are the general-purpose bipolar transistors, for instance, 2N2222 for Q2 and 2N2907 for Q3.

Output Capacitor Selection

For this application, there is a designed delay function to cause the overlap time between two sources when one source is turned on and the other turned off. The output capacitor here is not for holding up the supply, but for noise filtering and response to transient loading.

A widely used Electrolytic capacitor in 220μF or larger is recommended.

Conclusion

As discussed previously, Instantly Available PCs require unique Power Management devices to provide regulated voltage sources and intelligent switches between power sources.

This solution allows motherboard makers to distribute the power line to supply the SDRAM at every power saving state, which is also reducing the total BOM cost as the components are so easy to get in market.

Remove Q3 and R5 and connect pin 1 and Pin 2 of U2A, if 3.3V is not supplied at Soft-off.

Keep the output capacitor larger than 220uF to ensure the stability of the system and as close as possible to output line. It is highly recommended.

Please note that 74HCT00 would be recommended for the logical control due to fan-out issue.

Got any questions? Call AIC for applications assistance.

References

I. AIC1730 data sheet low noise 150mA LDO from Analog Integrated Corp.

II. MT18LSDT1672 SDRAM module data sheet from Micron Technology, Inc.

III. IAPC system power delivery requirements and recommendations Rev1.0 from Intel Corp.