

OCT8304B

Scaleable AAL2 Switching Using AAL2 Internal Transport

Application Note

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OVERVIEW

Voice over ATM (VoATM) is becoming more and more important in the carrier space as the convergence of voice and data networks progresses. Currently, the main application for VoATM is inter-switch trunking where considerable cost savings can be made by merging the traditional TDM network with the core ATM network. Moreover, we are observing new VoATM on-ramps with the deployment of DSL and next-to-come 3G wireless networks, creating VoATM traffic in the access as well as core portions of the ATM network.

The need for high-density AAL2 switching therefore arises and will become a vital function of any ATM network carrying AAL2 voice.

The following Application Note will describe how Octasic performs scaleable AAL2 switching with its OCT8304B AAL2 SAR.

AAL2 SWITCHING USING THE OCT8304B

General Description

The OCT8304B high-density AAL2 SAR is especially well suited to perform scalable AAL2 switching through an ATM switching matrix. Built around a linear architecture, it offers on one side a Utopia Level 2 interface for ATM transmissions and on the other a full H.100/H.110 interface which can be used to transport HDLC packets. To do this, the H.100 bus is subdivided into HDLC streams, up to 512, made of a concatenation of timeslots, increasing the bandwidth of the TDM interface for packet transmission.

The diagram in Figure 1 illustrates a Basic AAL2 Switching Module made of four OCT8304B AAL2 SARs used for AAL2 de-multiplexing and CPS packet re-encapsulation in AAL2 through HDLC. The traffic flow through these circuits is described in details in the next sections.

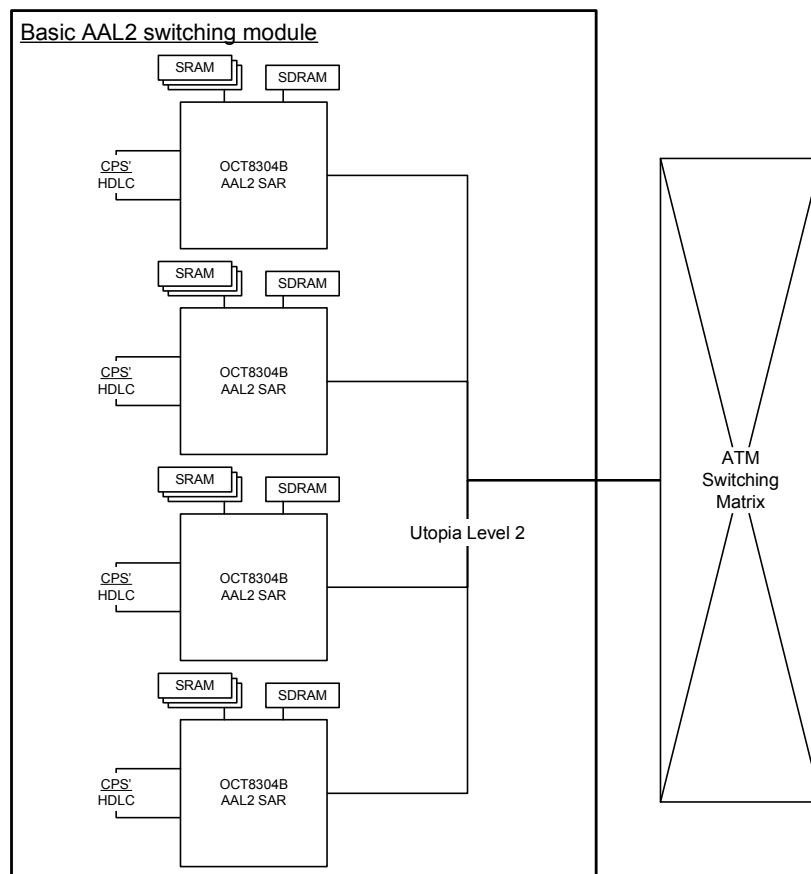


Figure 1 - Basic AAL2 Switching Module

The basic module of Figure 1 can be repeated any number of times on a board or in a system, making the solution scaleable until the switching matrix reaches the limits of its bandwidth or connection capacity. To that effect, some bandwidth calculations are made in the "Capacity Considerations" section below.

General Assumptions

The following assumptions are made throughout this document:

- All VPI/VCI parameters are considered internal to the architecture, in other words all network VCs terminated on a line card (characterized by a Port/VPI/VCI combination) have been translated to internal VCs characterized by unique VPI/VCI pairs inside the system before reaching any Basic AAL2 Switching Module.
- The term "channel" represents a duplex voice conversation and is characterized internally by a unique combination of VPI/VCI/CPS-CID parameters.
- All the CPS-INFO payload lengths range from 1 to 45 bytes, or 1 to 64 bytes, according to reference [2].
- Each internal VPI/VCI combination can carry up to 248 channels, or CIDs.
- The OCT8304B can inherently process no more than 155 Mbps of ATM bandwidth off of its Utopia Level 2 interface.
- Incoming traffic coming on the Utopia Level 2 interface has been smoothed by a traffic shaping function performed outside the Basic AAL2 Switching Module.
- All channels are considered to be already open by centrally-located or distributed control software, and processing traffic. Signaling of the entire AAL2 switching system can be performed in a number of ways (for example Q.2630.1) and is outside the scope of the document.
- The backplane ATM switching matrix Utopia connections facing the Basic AAL2 Switching Modules can operate as multi-PHY masters for at least four devices.

CPS Traffic Flow

The AAL2 switching function for CPS packets can be decomposed into two parts:

1. Ingress channel separation, where multi-channel AAL2 traffic flows from a line interface in the switching matrix, through one of the OCT8304B where its channels are de-multiplexed and then looped-back in HDLC format, re-encapsulated individually into AAL2 internal cells on a unique VC per channel pointing towards an egress AAL2 Switching Module.
2. Egress channel multiplexing, where reversely the single-channel AAL2 traffic flows from the switching matrix into one of the OCT8304B on the AAL2 Switching module, is looped-back on the HDLC interface and multiplexed into multi-channel VCs before being re-injected into the switching matrix towards a line interface.

These functions are explained in more details in the next sections.

Ingress Channel Separation

The ingress channel separation serves the purpose of breaking down the incoming multi-channel AAL2 VCs into their individual channels and forwarding the resulting CPS packets individually to their right egress port to be multiplexed back into multi-channel AAL2 VCs. The Ingress Channel Separation task is performed in two stages:

1. Stage 1: CPS packet separation and identification
2. Stage 2: HDLC CPS' packet encapsulation into single-channel AAL2 cells

Figure 2 below illustrates the ingress channel separation function for a portion of a basic AAL2 switching module, the other portions being symmetrical.

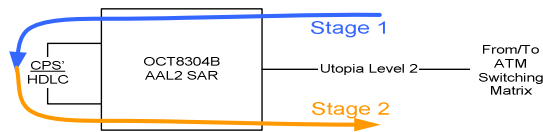


Figure 2 - Ingress Channel Separation

Stage 1 – CPS packet separation and identification

Incoming internal ATM/AAL2 cells from the switching matrix carry multiple channels as specified in reference [2], each channel uniquely identified by the CPS-CID parameter within its VPI/VCI.

Generally speaking, the OCT8304B can take multi-channel AAL2 cell streams and separate them into their individual CPS packets. Those are then written in HDLC format on the chip's HDLC interface.

More specifically, upon receiving AAL2 cell streams on its Utopia interface, the OCT8304B will perform the following functions:

1. For each ATM cell, identify the VC through a VPI/VCI lookup.
2. For each VC, separate the CPS mini-packets from the AAL2 cells and lookup their CID.
3. Based on CID and UUI, map each channel to a unique HDLC channel (stream and address) specified when the channel was opened.
4. Place a modified version of the CPS packets, (CPS' packets – illustrated in Figure 3 below) in the corresponding HDLC output buffer to be sent on the HDLC interface.

The HDLC packets generated by the OCT8304B are made of a header that contains 2 address bytes, as well as a possible control byte. There is also an optional 16-bit CRC that may be added at the end of the packet.

When converting AAL2 to HDLC, the OCT8304B outputs a modified version of the CPS packet (CPS'). In CPS', only the CPS-UUI byte is kept in the HDLC packet, carried over just before the first byte of the CPS-INFO payload. This allows the OCT8304B to remap the CID and LI and to recalculate the HEC when processing the channel in the other direction, e.g. during the egress channel multiplexing part explained in the next section. The following figure illustrates the CPS'/HDLC packet format:

	b7	b6	b5	b4	b3	b2	b1	b0
+0	Header							
+1	Header							
+2	Control (optional)							
+3	UUI							
+4	Payload (D0)							
+5	Payload (D1)							
	...							
	Payload (Dn)							
	CRC 0 (optional)							
	CRC 1 (optional)							

Where $0 \leq n \leq 44$

Figure 3 - HDLC-encapsulated CPS' packet

Stage 2 – HDLC CPS' packet encapsulation into single-channel AAL2 cells

Once written on the HDLC bus, the HDLC-encapsulated packets are read back instantly by the OCT8304B, which will perform the following functions:

1. Read the HDLC packets from the HDLC bus and regenerate a Length Indicator (LI) based on a payload count.
2. Look up the combination of HDLC stream and address and map the result to a CPS-CID and internal VPI/VCI.
3. Calculate a new CPS-HEC.
4. Place the newly formed CPS packet in the proper VPI/VCI FIFO queue.
5. Encapsulate the CPS packets present in the queue into single-channel AAL2 cells and output them on the Utopia interface towards an egress port.

Egress Channel Multiplexing

The egress channel multiplexing function is symmetrically opposite to the ingress channel separation function, and serves the purpose of re-mapping individual CPS packets carried inside single-channel AAL2 cells, into multi-channel AAL2 VCs. As before, the egress function happens in two stages:

1. Stage 3: Single-channel AAL2 conversion to HDLC
2. Stage 4: CPS' packets multiplexing multi-channel AAL2 cells

Figure 4 below illustrates the Egress Channel Multiplexing function.

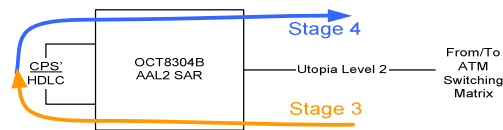


Figure 4 - Egress Channel Multiplexing

Stage 3 – Single-channel AAL2 conversion to HDLC

Upon receiving single-channel AAL2 cells, the OCT8304B performs the following:

1. For each ATM cell, identify the VC through a VPI/VCI lookup.
2. For each VC, extract the CPS mini-packet from the AAL2 cell and lookup their CID.
3. Based on CID and UII, map each channel to a unique HDLC channel (stream and address) specified when the channel was opened.
4. Place a modified version of the CPS packets, (CPS' packets – illustrated in Figure 3) in the corresponding HDLC output buffer to be sent on the HDLC interface.

Stage 4 – CPS' packets multiplexing multi-channel AAL2 cells

In stage 4, the OCT8304B will perform the following functions:

1. Read the HDLC packets from the HDLC bus and regenerate a Length Indicator (LI) based on a payload count.
2. Look up the combination of HDLC stream and address and map the result to a CPS-CID and egress VPI/VCI.
3. Calculate a new CPS-HEC.
4. Place the newly formed CPS packet in the proper VPI/VCI FIFO queue.
5. Multiplex the CPS packets present in the queue into multi-channel AAL2 cells and output them on the Utopia interface.

Delay Considerations

The table below shows the maximum delays that can be incurred at each stage.

Stage	Maximum Delay	Comments
1	250 μ s	Maximum delay incurred in the OCT8304B
2	250 μ s	Maximum delay incurred in the OCT8304B
3	250 μ s	Maximum delay incurred in the OCT8304B
4	250 μ s	Maximum delay incurred in the OCT8304B
Total	1 ms	

Note: Switching delays in ATM Switching Matrix are not included.

Capacity Considerations

The channel capacity of a Basic AAL2 Switching Module can be limited by one or more of the following factors:

- Channel capacity of the OCT8304B (maximum AAL2-to-HDLC channels processing capability)
- H.100 total HDLC bandwidth (2048 timeslots @ 64 kbps = 131 Mbps)
- Maximum bandwidth that can be processed on the OCT8304B network interface (maximum 155 Mbps of ATM traffic)
- Bandwidth of the Utopia Level 2 connection (622 Mbps)

The table below provides capacity guidelines for different CODEC profiles, assuming that 100% of the channels processed in the system are the same.

Codec	G.711	G.711	G.726	G.726	AMR*	AMR*
Rate (kbps)	64	64	32	32	12,2	7,4
Payload Length (bytes)	40	44	40	44	31	19
Packet Interval (ms)	5	5,5	10	11	20	20
OCT8304B internal bandwidth*	1212	1244	2424	2488	6120	6370
HDLC Bandwidth on H.100 bus**	1452	1472	2905	2945	7186	10503
AAL2 bandwidth on 155 Mbps Utopia**	1731	1743	3463	3485	8759	13537
Maximum number of channels processed in half module	1452	1472	2905	2945	7186	10503
Maximum number of channels processed in full module	2905	2945	5810	5890	14372	21005

Table 1 - Basic AAL2 Switching Module Channel Capacity

* Figures valid for a quarter module

** Figures valid for a half module

To support the current AAL2 Switching architecture, an ATM switching environment would have to support a large number of internal VCs within a system.

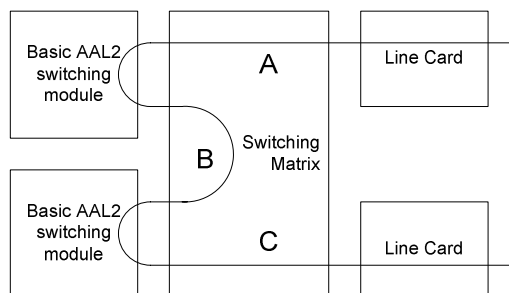


Figure 5 - Internal VC mapping

The total number of internal VCs in the system can be calculated by adding internal VCs at points A, B and C in Figure 5.

$$VC_{Tot} = VC_A + VC_B + VC_C$$
$$VC_A = \frac{ChCap}{\#Ch / VC_A} \times \# AAL2Modules$$
$$VC_C = \frac{ChCap}{\#Ch / VC_C} \times \# AAL2Modules$$

Where:

- VC_{Tot} is the total number of internal VCs in the system
- VC_{A,B,C} is the number of internal VCs at points A, B and C in the system
- ChCap is the target channel capacity for the system
- #Ch/VC_{A,C} is the amount of CPS channels carried inside internal VCs at points A and C
- #AAL2Modules is the total number of AAL2 modules in the system

At point B, the number of internal VCs can be calculated according to two different scenarios:

1. Internal VCs are statically assigned
2. Internal VCs are dynamically assigned

In the first scenario, we have:

$$VC_B = \# AAL2Modules \times ChCap$$

Whereas in the second scenario, we have:

$$VC_B = ChCap$$

As an example to illustrate the above calculations, if we want to switch 48,000 channels (full-duplex) of AMR 12.2 kbps in a system, you would need a total of four Basic AAL2 Switching Modules according to Table 1. At an average of 128 channels per multi-channel VC, in a dynamically switched environment, you would require:

$$VC_A = VC_C = \frac{48,000}{128} \times 4 = 1500$$
$$VC_B = 48,000$$
$$VC_{Tot} = VC_A + VC_B + VC_C = 1500 + 1500 + 48,000$$
$$VC_{Tot} = 51,000$$

REFERENCE LIST

- [1] Recommendation I.361, B-ISDN ATM layer specification, 1995, International Telecommunications Union
- [2] Recommendation I.363.2, B-ISDN ATM Adaptation Layer (AAL) type 2 specification, Nov 2000, International Telecommunications Union
- [3] OCT8304DS8000 - OCT8304 Specifications, Octasic Inc.

REVISION CONTROL

Revision	Date	Changes
1.0	March 2002	First release

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