

Protecting Against Unintentional Writes When Using Single Power Supply Flash Memories



Application Note
Revised March 1999

1.0 INTRODUCTION

Single power supply reprogrammable nonvolatile memories have all the benefits of a single power supply device, but there is a concern that must be addressed by the user. Since single power supply reprogrammable nonvolatile memories, e.g., SST SuperFlash EEPROMs, are intended to be altered in-system with the use of one power supply, e.g., similar to SRAMs, there exists the possibility of unintentional writes. The means to avoid unintentional writes are described below.

Unintentional writes can be of two categories:

- False write occurs during an intentional write cycle, when either the data loaded or the page address loaded is wrong. False write can be minimized by following the hardware design recommendations to be described later. False write failures are generally not repeatable and occur as unique events when writing.
- Inadvertent write occurs by unintentionally issuing a valid Write command, i.e., the Write command is executed by noise or by uncontrolled signals, usually during power-up or power-down. Inadvertent write is normally eliminated by using SDP. The hardware design recommendations can also help reduce inadvertent writes.

Dual power supply device applications, that remove the second high voltage supply when not writing, generally alleviate the concern with inadvertent write, although false write may still occur.

2.0 False Write Protection

False writes are minimized by following standard PCB design practices. Since false writes are normally caused by noise on the V_{SS} line, the noise emanating from switching the voltage/current of some signal. SST recommends a high frequency 0.1 μF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS} , e.g., less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 μF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 5 cm of the V_{DD} pin.

Note: V_{DD} is the 5 volt power supply. For a 5 volts nominal level, V_{DD} is often called V_{CC} . For other nominal values, e.g., 3 volts, the JEDEC defined term is V_{DD} .

A 3.3 K-ohm pull-up resistor on WE# reduces transients on WE#, when WE# is toggling to load address or data; thus, minimizing the possibility of loading the incorrect data or address. The pull-up resistor should be connected from WE# to V_{DD} , as close as possible to both pins. Should a CE# controlled Page-Write cycle be used instead of WE# controlled, then the pull-up resistor should be on CE#.

SST recommends that during a WE# controlled write cycle that CE# be held low and OE# be held high, instead of toggling. Again this minimizes transients that generate noise.

3.0 Inadvertent Write

Inadvertent write generally occurs during a power-up or power-down when the system provides a valid, yet unintentional write command. There are two major methods of reducing this possibility:

- Power-up and power-down sequencing assures the device will not have the control logic at the proper levels to initiate a write. The recommended sequence for devices using WE# controlled writes during power-up is WE#, V_{DD} , CE#, OE#. Note, with the pull-up resistor on WE#, WE# will automatically track V_{DD} . The recommended power-down sequence is the reverse; OE#, CE#, V_{DD} , WE#.
- The most effective method is the use of Software Data Protection (SDP). Once enabled, the device is protected from noise transients affecting the control, address, and data lines during a power-up or power-down. SDP requires the use of a 3-byte sequence (or to disable protection, which SST does not recommend), to alter the device once protection is enabled.



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The SDP Enable command and the SDP Write command are identical, so the very first write to the device should use the SDP sequence. Every subsequent write then uses the exact same 3-byte sequence to initiate the write to each page. Only the page loaded will be written, all other pages are secure from false or inadvertent writes (use of the above described hardware protection methods assures only the correct page will be loaded). SDP provides a level of write protection similar to that provided by the second high voltage power supply in some flash memories, without the cost and inconvenience of providing and switching a high voltage supply.

4.0 Summary

The protection methods, both hardware and SDP, described above, when employed in the application will prevent unintentional writes. SST SuperFlash EEPROMs, employing SDP and with the board design recommendations described, provide the highest level of data security and protection with all the benefits of single power supply flash memories.