



# SST's MTP Products

## A Superior Alternative to EPROM and Low Functionality Flash

Application Note

### 1.0 Introduction

MTP is a Many-Time Programmable low cost flash memory. The MTP combines the electrical erasability of flash and the cost effectiveness of EPROM. SST designed the MTP products, a low cost NVM, by reducing some of the peripheral circuitry of existing high-functionality SuperFlash products while retaining the benefits of the SuperFlash core – higher reliability, faster write performance, geometric scalability, and a low-cost manufacturing process.

This application note describes the features and benefits of SST's MTP products and how they can be used in existing UV-EPROM, OTP, and flash designs. The contents of this application note will apply to all MTP product densities.

### 2.0 Device Operation

MTP products are functionally (Read and Program) compatible with industry standard UV-EPROM and OTP products utilizing the same timing and pinouts. MTP supports electrical Erase operation instead of ultraviolet Erase in UV-EPROMs.

MTP products with densities of 2M or lower will be offered either at  $V_{CC} = 5.0V$  or  $2.7V$  Read, while 4M densities will be offered only in  $2.7V$ . All MTP devices are programmed and erased with  $V_{PP}$  at  $12V$ . For Read operation,  $CE\#$  and  $OE\#$  have to be held low and the output data then becomes available after the standard access time. The MTP device is programmed byte by byte and is erased by a Bulk Erase operation. Both Program and Erase operations are hardware-controlled operations at room temperature. Unlike other flash, MTP does not use SDP (software data protection) command sequences for initiating Program or Erase operations. The 1M and 2M MTP devices are programmed and erased using a single pulse on the  $PGM\#$  pin ( $PGM\# = V_{IL}$ ). The 256K/512K/4M devices are programmed and erased using a single pulse on the  $CE\#$  pin ( $CE\# = V_{IL}$ ). The falling edge of  $PGM\#$  or  $CE\#$  (whichever applies) initiates the Program/ Erase operation. The MTP device requires  $20\ \mu s$  per byte for Program and  $100\ ms$  for bulk Erase operation. The Erase mode is distinguished from the Program mode in all the above cases by applying an additional voltage of  $12V$  to the  $A_9$  pin. The  $OE\#$  signal is  $V_{IH}$  in all cases, except for the 512K device where  $OE\#$  is a dual-function  $OE\#/V_{PP}$  pin and requires  $12V$  for Program/ Erase operation. The control signals applied are given below. For more details on device operation, please refer to the appropriate MTP datasheet.

### Program

For 1M/2M  $CE\# = PGM\# = V_{IL}$ ;  $V_{PP} = 12V$ ;

( $PGM\#$  requires a pulse of  $20\ \mu s$ )

For 256K/512K/4M  $CE\# = V_{IL}$ ;  $V_{PP} = 12V$ ;

( $CE\#$  requires a pulse of  $20\ \mu s$ )

### Erase

For 1M/2M  $CE\# = PGM\# = V_{IL}$ ;  $V_{PP} = A_9 = 12V$ ;

( $PGM\#$  requires a pulse of  $100\ ms$ )

For 256K/512K/4M  $CE\# = V_{IL}$ ;  $V_{PP} = A_9 = 12V$ ;

( $CE\#$  requires a pulse of  $100\ ms$ )

### 3.0 Benefits of SST's MTP Products

#### 3.1 Greater functionality with electrical erase and reprogrammability

MTP products provide greater functionality that make them better alternatives to standard EPROM products. Standard UV-EPROMs require a separate UV Erase operation, while OTP can only be programmed once. If an OTP solution is used, all inventory that requires a subsequent bug fix or a software upgrade would have to be discarded, therefore adding to inventory costs. An MTP solution used would eliminate such added inventory costs, since an MTP device could be quickly erased and reprogrammed. Total cost of ownership associated with MTP solutions is therefore inherently lower than that of either UV-EPROM or OTP solutions.

#### 3.2 Faster Program and Erase

One of the biggest advantages of MTP is the faster total program and erase time compared to EPROMs and low functionality flash. The comparisons below are made with reference to 1 Mbit devices.

- OTPs take a minimum of  $100\ \mu s$ /byte to program an entire chip. Therefore, a 1 Mbit OTP device will take about 13.1 seconds to program the entire chip, and it is programmable *only once*.
- UV-EPROMs require an UV-eraser and about 30 minutes to erase the chip and  $100\ \mu s$ /byte to program. Therefore, 1 Mbit UV-EPROM device would take a total of over 30 minutes to both erase and program.



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- The 1 Mbit bulk-erase flash takes a minimum of 10 seconds for a chip erase and 12.5 seconds for a chip program. Note, in the case of Erase, the above numbers do not include the time taken to pre-program every location to 00H – a process that is required to avoid the overerase problem of bulk-erase flash that SuperFlash technology inherently eliminates. Another point worth noting is that Erase and Program times for bulk-erase flash get longer with additional endurance cycles.

In contrast, a 1 Mbit MTP device can be electrically erased in a *maximum* of 0.1 seconds and reprogrammed in about 2.6 seconds (without requiring any pre-programming to 00H), therefore having a shorter re-program time than any of the above NVM solutions.

The faster Program and Erase operations result in lower manufacturing cycle times resulting in lower manufacturing costs. Testing times and testing costs are also reduced as a result of faster erase and programming times. In addition, faster Program and Erase operations will also reduce development cycles and improve time to market. MTP has a clear advantage when compared to EPROMs and low functionality bulk-erase flash.

### 3.3 Lower Cost NVM Solution

Many applications do not require all of the enhanced features of high functionality flash, such as single power supply and smaller sector architecture, but still require the insurance of re-programmability. However, until now, industry has used higher cost flash due to the lack of an appropriate NVM solution. In order to address these applications, SST designed lower cost NVM solutions by eliminating some of the peripheral circuitry of existing SuperFlash high functionality flash products like charge pump, SDP circuitry, and circuitry for small sectors. Consequently, in those applications where enhanced flash functionality is not needed, MTP provides the above applications with a low cost alternative NVM.

Since MTP does not use UV erase, windowed packages are not needed. This allows MTP to be offered in a cost-effective plastic package such as PDIP and PLCC. A UV-EPROM, on the other hand, requires a windowed package that allows UV light, resulting in higher packaging costs. OTP has a higher cost of manufacturing when compared to MTP, due to its higher yield loss due to programming errors. With MTP, the yield loss due to programming errors is zero, since MTP can be quickly erased and reprogrammed.

### 3.4 Uses Superior SuperFlash Technology

MTP products are based on SST's core SuperFlash technology and inherit all the benefits associated with this superior technology. SST's proprietary memory cell design uses relatively thick oxides compared with other flash technologies. The SuperFlash tunnel oxide is three to four times thicker than conventional flash tunnel oxide, resulting in excellent data retention (100 years), thus higher reliability than conventional flash (10 years).

For erase, SST's SuperFlash memory cell uses an average electric field of 4MV/cm, as opposed to 10MV/cm in conventional flash, which increases the possibility of oxide rupture on conventional stacked-gate flash memory.

SST's Split gate design isolates each memory cell from the bit line, eliminating any possibility of overerase failures. Conventional flash, on the other hand, requires special circuitry to reduce overerase. In addition, in conventional flash, every location needs to be pre-programmed to 00H prior to erase. This results in a slower Erase operation for conventional flash memory.

The cost of flash memory is primarily a function of wafer fabrication and testing. Unlike conventional flash technology, SST's SuperFlash technology uses a simple process with fewer masking layers, significantly reducing the cost of wafer manufacturing and resulting in higher yields. As seen earlier, the testing time and costs are reduced by the faster Program and Erase cycles.

### 3.5 Choice of NVM Solutions from SST

With introduction of MTP products, SST will provide complete NVM solutions to system designers. The system designer may use SST's 29EExxx page mode EEPROM for higher functionality or MTP products for lower cost NVM requirements.



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#### 4.0 Compatibility between EPROM and MTP

MTP devices are offered in the same packages as OTP and UV-EPROM devices. They are pin-to-pin compatible in all package types. Therefore, no changes in board layout are needed. The 1, 2, and 4 Mbit products are available in 32-pin PDIP, PLCC and TSOP packages, while the 256 and 512 Kbit products are offered in 28 pin PDIP and TSOP and 32 pin PLCC packages. The Read operation of both EPROMs and MTP are identical. The difference in programming algorithm is transparent to end users since Program or Erase operations are normally performed using an external programmer.

#### 5.0 Compatibility between MTP and Bulk-Erase Flash

SST's 1 and 2 Mbit MTP devices are offered in the same packages as other 1 and 2 Mbit Bulk Erase flash devices – 32-pin PDIP/PLCC/TSOP packages. They are pin-to-pin compatible in all package types except for the WE# pin on flash and PGM# pin on MTP. However, these two pins are used for Program or Erase operation, as described in Section 2.0 of this application note. There would be no impact on system design or layout if programming was done using an external programmer. For the same reason, difference in programming algorithm is transparent to end users. As a result, MTP can be used as a 100% drop-in substitute in the 1M and 2M densities, without any board layout modifications.

In the case of the 256K and the 512K, EPROM and flash have different pinouts. This is why MTP at these densities is not pin to pin compatible with flash, and therefore, small layout changes would be required.

#### 6.0 Programmer Support

All MTP products will have programmer support from leading programmer vendors. Please contact SST or local SST representative to obtain the list of programmer support available for MTP products.

#### 7.0 In-System Programmability (ISP) Issues

MTP is mainly suitable for applications that do not require in-system programmability (ISP). However, an MTP device may be programmed in the system if a 12V supply is available on the system.

The system design should include a jumper to switch the A<sub>9</sub> pin between Address pin and the 12V V<sub>PP</sub> pin. This is because the A<sub>9</sub> pin is a dual-functionality pin that is used as address input during program and high voltage pin during erase. It should be noted that for all MTP devices, temperature condition should be 25°C±5°C for program and erase operations. Also, de-coupling capacitance is required on V<sub>CC</sub> and V<sub>PP</sub>, so that any noise on V<sub>CC</sub> or V<sub>PP</sub> during Program/Erase is filtered. As a result, the Program/Erase operation does not get intermittently disabled by noise when memory locations are being erased or programmed.

Another difference between MTP and flash will be the use of software command sequences for flash which is not used by MTP products. Therefore, software command sequences used to program flash need to be bypassed when programming and erasing MTP products in the system.

#### 8.0 Conclusion

MTP combines the electrical erasability of flash with the cost effectiveness of EPROMs. This makes MTP a cost-competitive NVM solution vs. EPROM and other flash applications where ISP is not required. The pin compatibility of MTP with EPROM supports 100% drop-in replacement and provides a cost reduction for existing systems that utilize EPROM. As a result, MTP provides the NVM market with a low cost alternative to bulk-erase flash and a high functionality alternative to EPROMs.



# SST's MTP Products

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