

SST89F5x Oscillator Circuit Design Considerations



Application Note
August 1999

1.0 Introduction

The SST89F5x FlashFlex51 Family of microcontrollers has two modes of clock options: On-chip oscillator and external clock drive. This application note provides oscillator circuit design considerations for the On-Chip oscillator mode.

2.0 On-Chip Oscillator

XTAL1 and XTAL2 are the input and output of an inverting amplifier as shown in Figure 1 below. The internal feedback resistor, R_f , biases the inverter in its linear region and forms a closed loop feedback system. A quartz crystal along with a pair of loading capacitors makes up the external portion of the oscillator circuit. An optional series resistor, R_s , may be used to limit the overall gain if the crystal is being overdriven.

3.0 External Components Selection

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 1 suggests some typical values for C1 and C2 at a given frequency. If, following the satisfactory selection of all external components, the circuit is still being overdriven, a series resistor, R_s , should be added. If there is voltage clipping between V_{DD} and V_{SS} , that is usually a good indication that the crystal is being overdriven.

TABLE 1. RECOMMENDED COMPONENTS VALUES

Frequency	C1 and C2	R_s (Optional)
< 8 MHz	90 - 110 pF	100 Ω
8-12 MHz	18 - 22 pF	200 Ω
> 12 MHz	18 - 22 pF	200 Ω

4.0 Amplifier Gain

The oscillator circuit consists of an amplifier and a feedback network. In order for oscillation to commence, two conditions must be met: 1) the overall loop gain must be greater than unity. 2) The phase shift must be 0° or 360° . The loading capacitors C1 and C2 must be properly selected to ensure these above conditions are met.

5.0 Stability

Stability is achieved once the oscillator is resonant at the desired frequency. Various parameters affect frequency stability but not all are critical. Some parameters a designer should consider are: Temperature, drive level, crystal aging, crystal tolerance and deviation over temperature and frictional wear. Increasing C1 and C2 will improve frequency stability by limiting the drive level, but that also increases startup time. Instead of increasing C1 and C2, use a series resistor, R_s , to reduce the drive level.

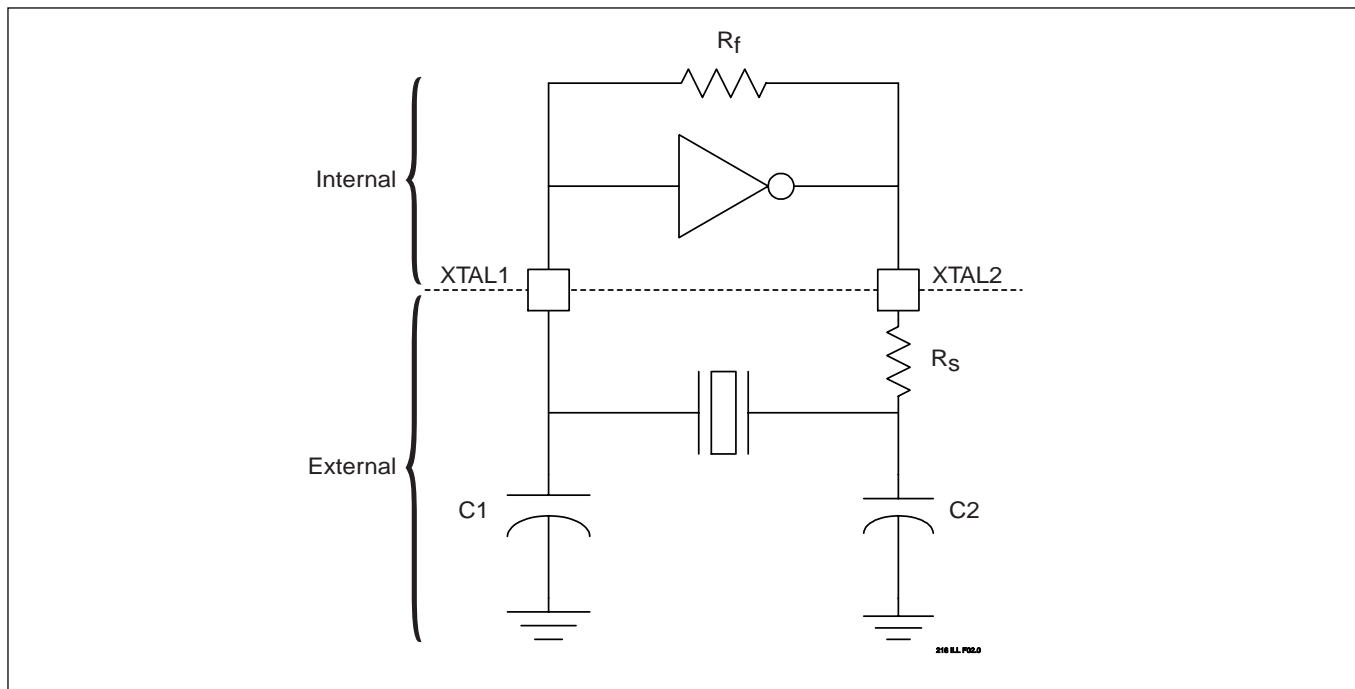


FIGURE 1: ON-CHIP OSCILLATOR

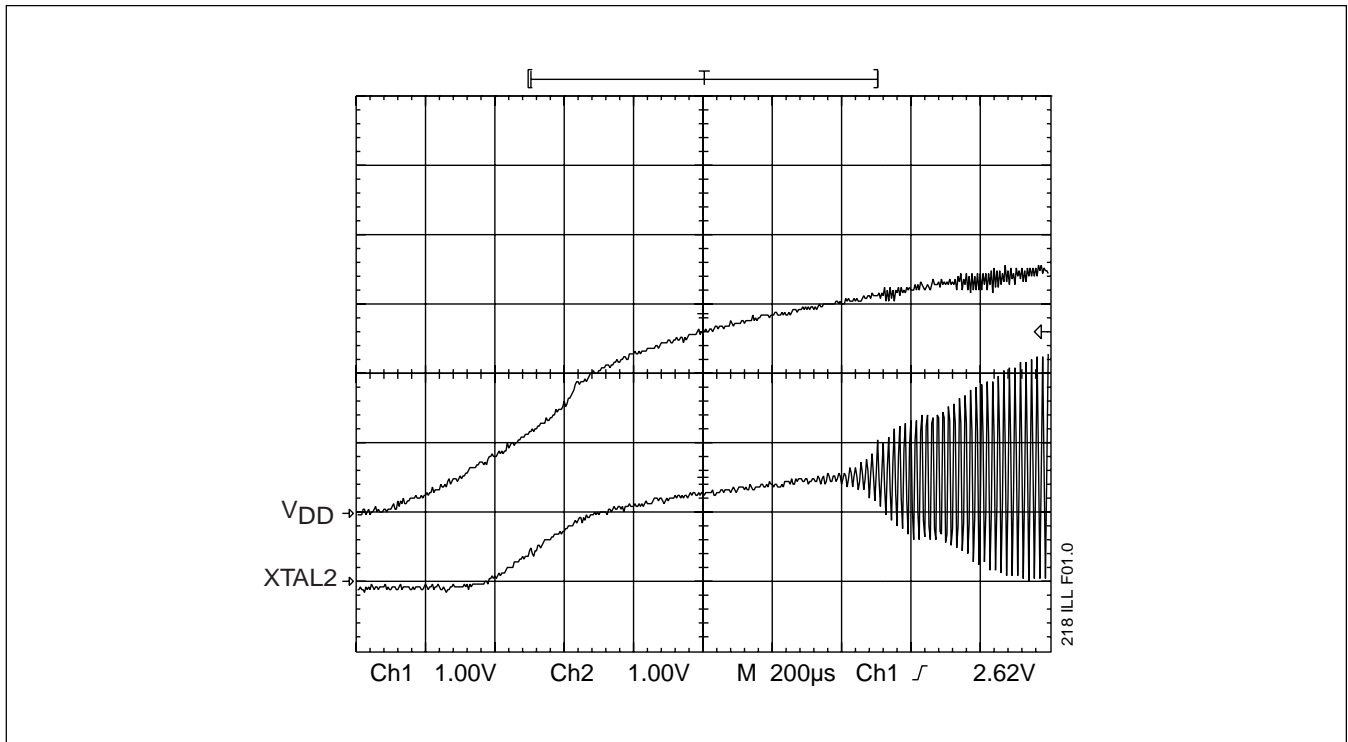


FIGURE 2. OSCILLATOR STARTUP FOR A 11.0592 MHz CRYSTAL

6.0 Startup Time

Startup time is critical in an oscillator circuit because of the microcontrollers reset and initialization requirements. Most crystal oscillator circuits typically take between 0.5 to 5ms to startup. Figure 2 shows the startup time for an 11.0592 MHz crystal oscillator circuit. For a low frequency crystal, the startup may take up to several seconds. The latency in startup time can disrupt the Power-on Reset process. To ensure a proper reset, the oscillator must be stable for at least two machine cycles (24 clocks) after achieving stable resonance. Therefore, for a low frequency crystal, it is necessary to extend the reset signal to avoid an invalid reset.

The loading capacitors C1 and C2 should be kept small to minimize startup time but robust enough to provide adequate gain for startup. A higher C2 value can increase the phase shift across the crystal at power-up and help increase the startup time.

5.0 Design Considerations

Certain design guidelines must be followed for a good oscillator circuit. Stray capacitances and large inductances must be kept to a minimum to avoid an undesired mode of oscillation and startup issues. A good practice is to keep all trace lengths as short as possible. Components should be isolated in order to prevent signal coupling. Ground planes should be used to isolate signals. Special precautions must be taken for single or double layer board designs with no ground planes. Additionally, a 0.1µF ceramic high frequency, low inductance capacitor connected between V_{DD} and Ground should be placed as close to the package terminals as possible to remove power line noise. Refer to the application note on *Design Considerations for the SST FlashFlex51 Family Microcontroller* for general PCB design guidelines.



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